TOSHIBA

FIE NO. 336-9612

TECHNICAL TRAINING MANUAL

3 LCD DATA PROJECTOR

TLP411U
TLP411E

Dec., 1996

CONTENTS

SECTION I
MAIN POWER SUPPLY CIRCUIT

1. OUTLINE

The power supply circuit operates on AC as input and outputs DC (+S6V, +6V, +10V, +12V, +15.5V) through inverter after rectification and smoothing of the AC power.

ON/OFF function is provided for outputs other than +S6V by the external signal. It is also capable of providing high voltage output with inverter drive for halogen lamp. Fig. 1-1 shows the block diagram.

1-1. Block Diagram

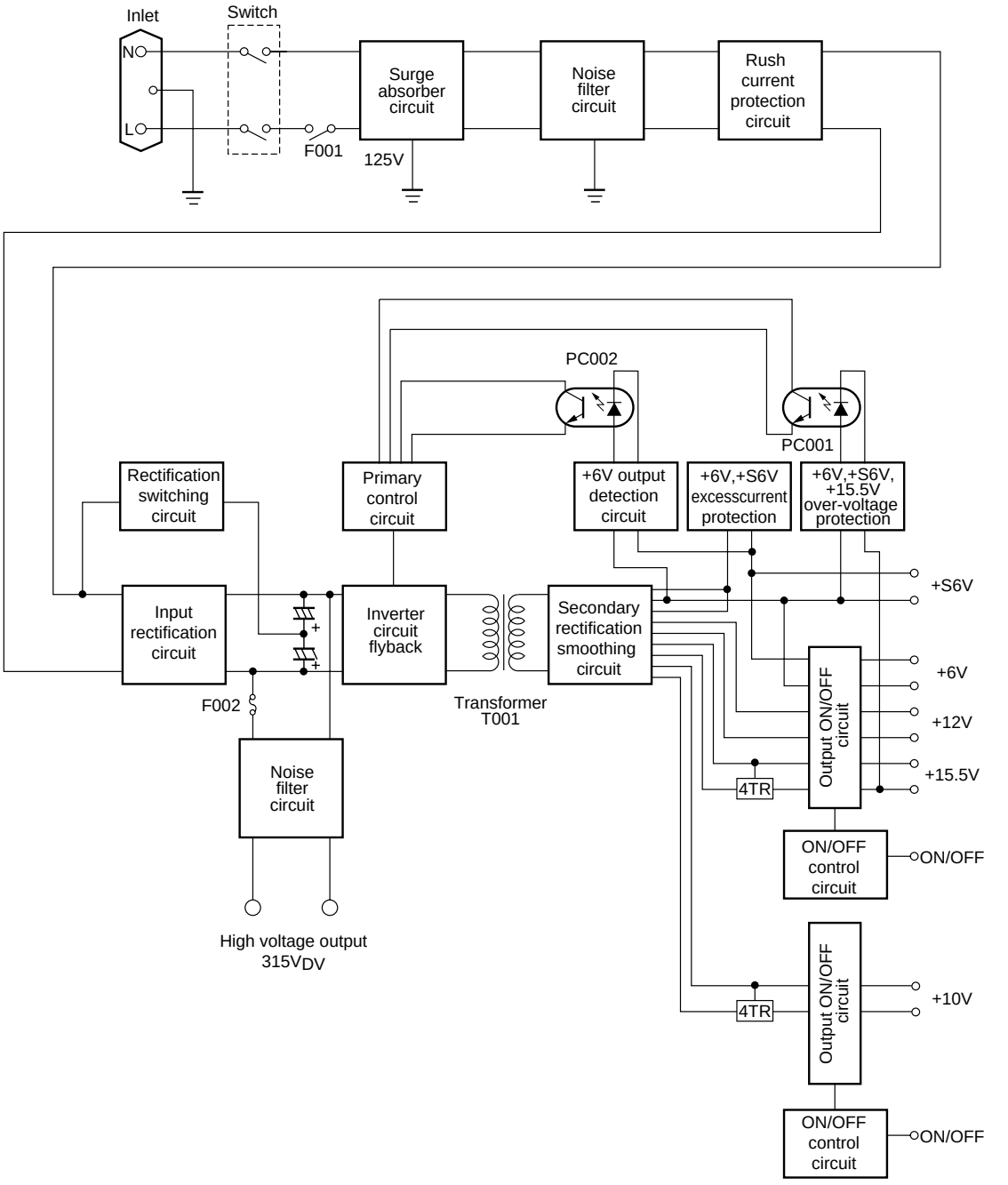


Fig. 1-1 Block diagram

2. DESCRIPTION ABOUT CIRCUIT OPERATION

2-1. Surge Absorber Circuit

The surge absorber circuit consists of protection element (varistor) and spark gap on the pattern surface on the PC board, making it possible to protect the power from being destroyed by lighting stroke and impulse invaded from external or from malfunction.

2-2. Noise Filter Circuit

The noise filter circuit only protects the noise generated by the power source from leaking out to AC line and from entering of the external noise inside the power. This circuit is effective for both normal and common noise.

2-3. Rush Current Protection Circuit

When AC power is, via D001, rectified and directly applied to C011 and C012, rush current runs through C011 and C012 as shown in Fig. 1-3. The current degrades the contact point of SW001. This rush current is controlled by the circuit shown in Fig. 1-2, preventing the degradation of the contact point.

Before the power activation, there exists no induced voltage in T001. SCR001 is in the OFF state. Rectified AC current runs through RF001 and charges C011 and C012.

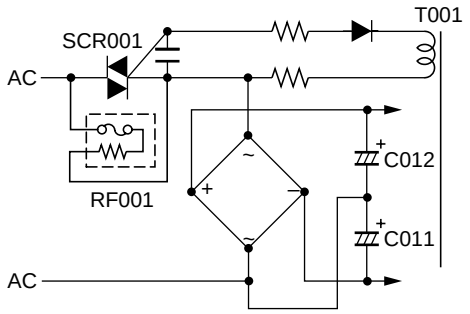


Fig. 1-2

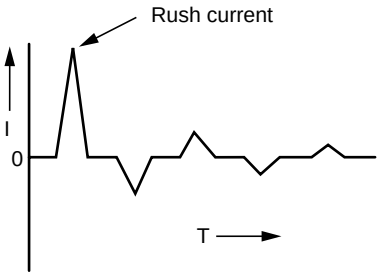


Fig. 1-3

With this, RF001 becomes charging resistance and is suppressed less than 30A. Then, when the charging voltage of C011 and C012 becomes more than the activation voltage, the inverter starts oscillation (activation) and the voltage is generated in the T001. This voltage is used for trigger voltage for SCR001, turns on the SCR001 and short-circuits the RF001. As a result, the rectified current flows into C011 and C012, eliminating the power loss by RF001 in the normal operation state.

2-4. Smoothing/Rectifying Circuit

The input voltage of the unit is set to work in the range of AC100 ~ 120V and AC220 ~ 240V. To keep the AC rectification output voltage in almost the constant level, the voltage doubler rectification is employed for the AC100 ~ 120V input and the bridge rectification for the AC220 ~ 240V input. An exclusive IC is used to switch the voltage doubler rectification and the bridge rectification. Figs. 1-4, 1-5 and 1-6 show the basic circuits.

When the switch is turned off, each of a positive and negative half-wave voltage of $V_{IN\ (AC)}$ is charged to C012 and C011, and the bridge rectification voltage is developed from the output terminal. On the other hand, when the switch is turned on, a positive half-wave voltage of $V_{IN\ (AC)}$ is charged to C012 through the circuit shown by ⟶ and a negative half-wave voltage of $V_{IN\ (AC)}$ is charged to C011 through the circuit shown by ⇢. The voltage doubler of the half-wave rectification voltage is developed from the output terminal.

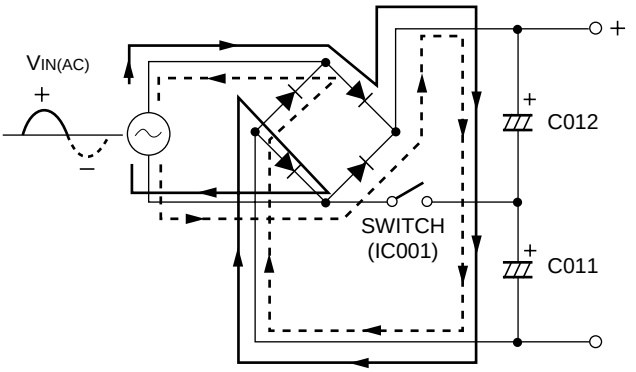


Fig. 1-4 Bridge rectification (SW: OFF)

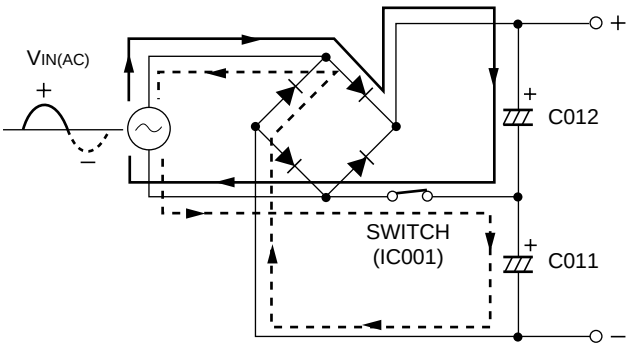


Fig. 1-5 Voltage doubler rectification (SW: ON)

The half-wave rectification for $V_{IN\ (AC)}$ is carried out by C and Di (D007) shown in the dotted line ----. When the input voltage is low, the triac is turned on (voltage doubler rectification) and when the input voltage high, the triac is turned off (bridge rectification).

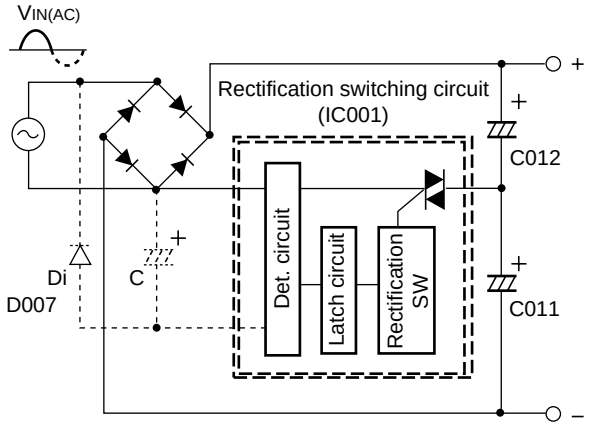


Fig. 1-6

2-5. Inverter Circuit (Flyback)

The current indicated with ⟶ to the converter transformer is turned on/off by the FET switch of Q001 operation. In the OFF state, the current indicated with ⇢ flows.

Signal is supplied to gate from the primary control circuit. With this, Q001 starts switching operation.

Gate voltage, drain voltage, and current waveform of Q001 are shown in Fig. 1-7.

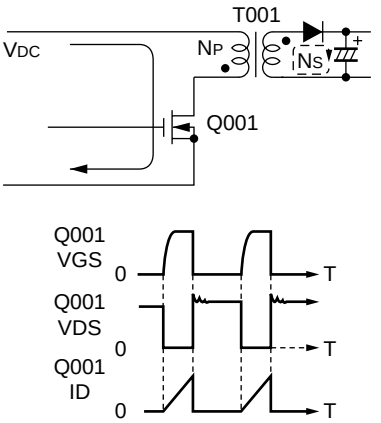


Fig. 1-7

2-6. Primary Control Circuit

The control system employs automatic flyback system by timing capacitor.

In the circuit diagram in Fig. 1-8, when power is turned on, input voltage V_{DC} is applied to B point. Voltage is applied to Q001 gate via R009 and R010. Then Q001 is activated. When Q001 is turned on, the drain current begins to flow as shown in Fig. 1-7 and input voltage is applied to N_P winding.

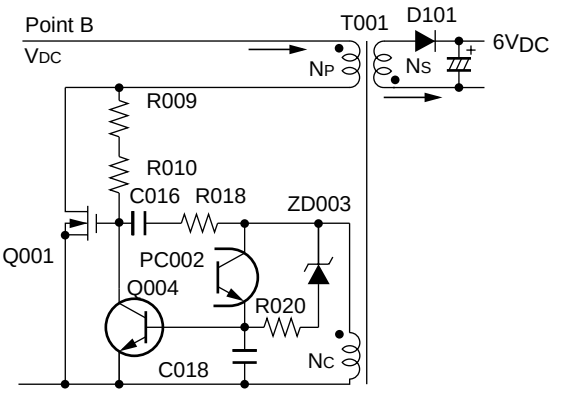


Fig. 1-8

The voltage $V_{NC} = N_C/N_P \times V_{DC}$ is generated in the N_C winding and voltage is supplied to Q001 gate through R018 and C016. At the same time, C018 is charged through ZD003 and R020.

When the electric potential of C018 rises up to V_{BE} (Sat) = approx. 0.7V, Q004 is turned on and Q001 is turned off.

That is, ON period of Q001 is determined by the time constant of ZD003, R020 and C018. When Q001 becomes off, the energy (flyback) accumulated in the transformer T001 is output through D101. When this energy becomes zero, D101 becomes off. For there exists a slight residual energy in N_S winding, by means of which voltage is generated in the gate winding N_C, which turns on the Q001 again to resume switching operation.

On the other hand, when the voltage output through D001 is rectified by the secondary rectifying/smoothing circuit, when the voltage is detected by +6V detection circuit, PC002 becomes on. This shortens the time constant to charge C018. At the same time, the ON period of Q001 is controlled and the output voltage (+6V) becomes stable.

2-7. Secondary Rectification & Smoothing Circuit

High-voltage applied to N_P becomes, as mentioned previously, pulse by means of the switching operation and then converted to low voltage at both ends of the secondary side winding N_S via T001 and is output after rectification/smoothing.

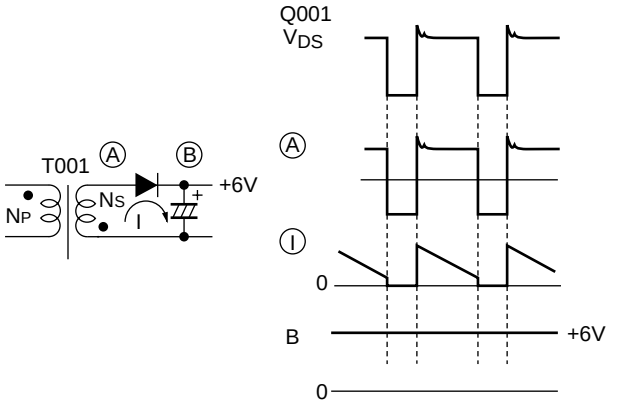


Fig. 1-9

2-8. +6V Detection Circuit

+6V voltage is divided by VR101, R113 and R114, it is input to the gate of IC101 and then it is compared with the reference voltage of that IC. This potential difference flows into PC002 as current variation which is then transferred to the primary side control circuit to control output voltage.

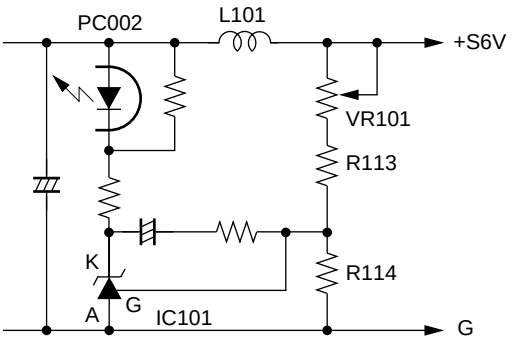


Fig. 1-10

2-9. +6V, +S6V, +15.5V Overvoltage Protection Circuit

As shown in Fig. 1-9, the overvoltage of +6V and +S6V is detected by ZD101 and the overvoltage +15.5V is detected by ZD401.

When the overvoltage is detected, current flows to zener diode, the current then flows to PC001. This is transferred to the primary control circuit and trigger signal is given to the gate of thyristor SCR002 to short-circuit the gate of Q001. As a result, Q001 turns off and the oscillation stops.

The circuit is put to the latch mode. Therefore, no activation is possible even overvoltage state is released. Activation is made possible by reentry of input.

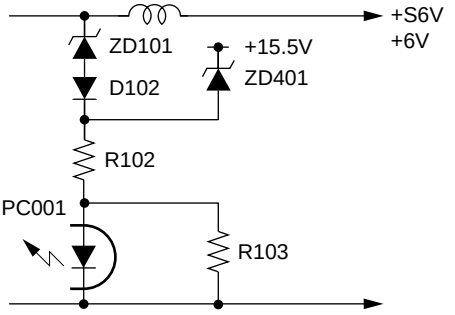


Fig. 1-11

2-10. +6V, +S6V Over Current Protection Circuit

As shown in Fig. 1-12, this circuit detects the over current by differential amplifier consisting of Q102 and Q103. The reference voltage is produced by voltage division of R105 and R106 using the +S6V as voltage source. This voltage called VA (+S6V x R106/R105 + R106) is compared with Voltage VB (Ioc x R108) generated by over current. Q101 and Q102 turn on under the VA < VB condition, by means of which the current is supplied to PC001. This is transferred to the primary control circuit. The rest of operation is the same as item 2-9.

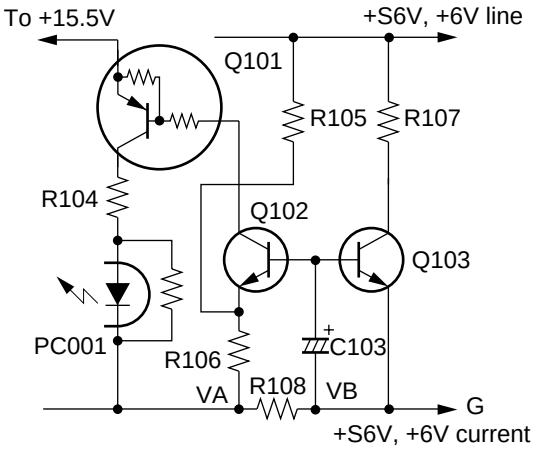


Fig. 1-12

2-11. Output ON/OFF Circuit

+15.5V and +10V outputs can be turned on/off by 4-terminal regulators IC401 and IC201. +5V and +6V outputs can be turned on/off by POWER MOSS FET (Q106, Q302). ON/OFF signal is given by the following ON/OFF control circuit.

2-12. ON/OFF Control Circuit

This circuit controls the circuit of item 2-11, which delays the external signal by the integration circuits (R118 and C108) to send signals to each output circuit. Signal level is TTL level. Each output becomes off at “L” and becomes on at “H” approximately 300 ms later.

The ON/OFF signal of +12V is input from pin 2 of CN104 and turns Q302 ON/OFF passing through Q301 and PC101.

SECTION II
LAMP HIGH VOLTAGE POWER SUPPLY CIRCUIT

1. LAMP HIGH VOLTAGE POWER SUPPLY

The lamp high voltage power supply receives a DC220 to 390V (primary side) from the system power supply and provides a DC voltage (50 to 70V_{DC} at ever turning on the lamp) to turn on the lamp. Fig. 2-1 shows the block diagram.

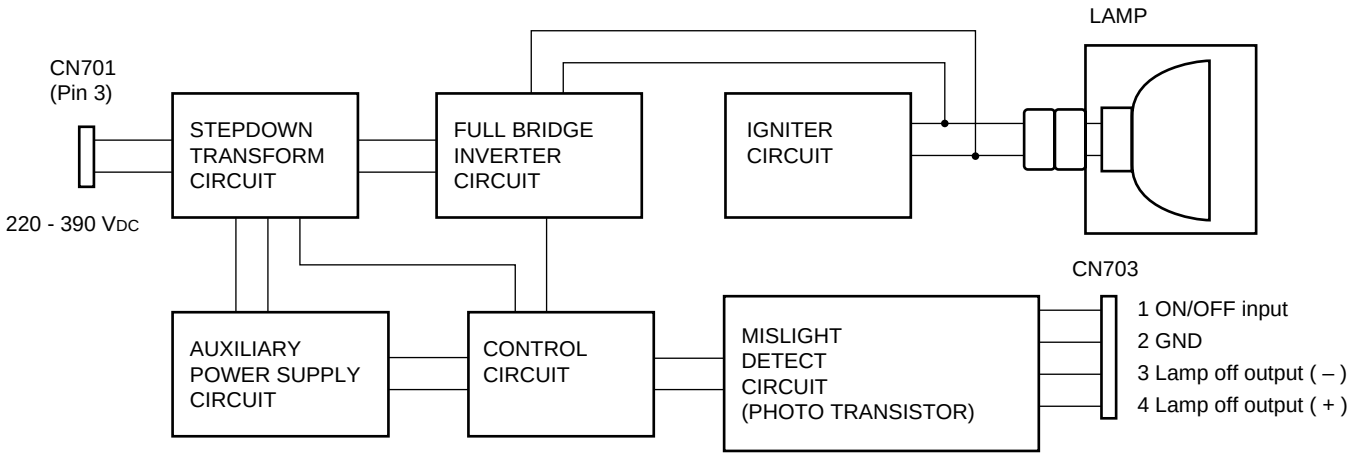


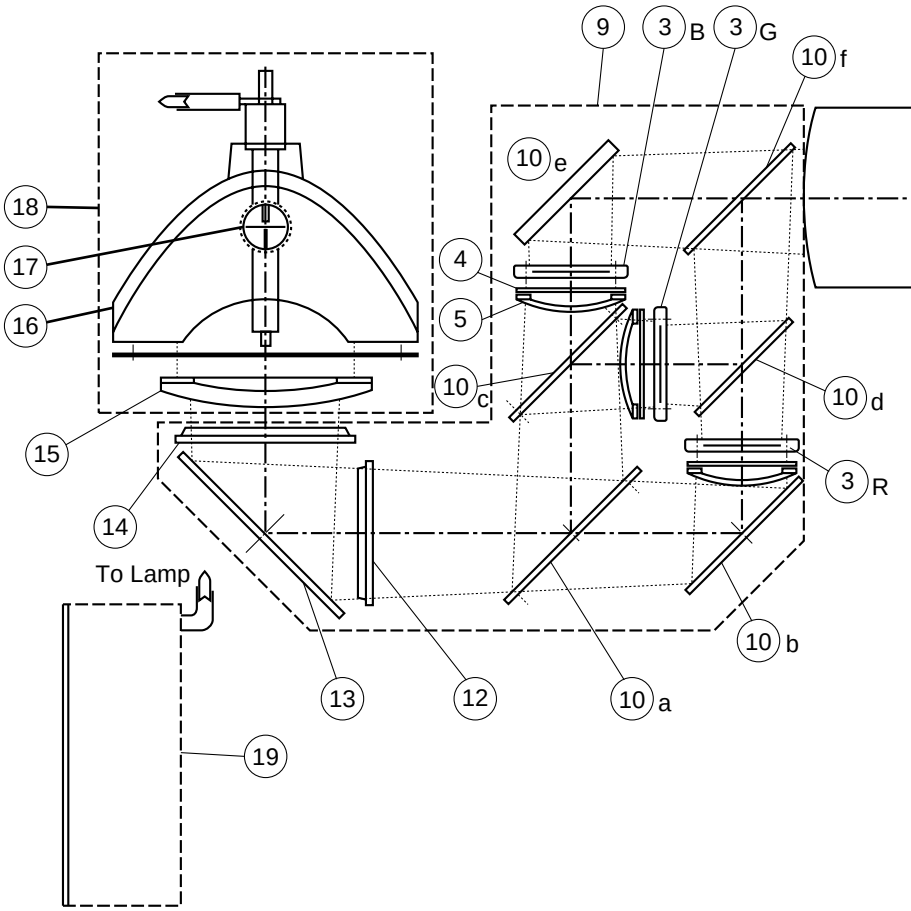
Fig. 2-1

The DC voltage is supplied to CN701 from the main power supply unit through an interlock switch (S023). This voltage becomes AC input x 2Ö2 (= 340V for AC120V input) when the lamp is off. CN703 is a connector for the lamp on control signal input and lamp off control signal output. When +5V is applied to the ON/OFF input in the standby on, Q702 FET transistor turns on, igniter develops a high voltage pulse (13 to 18 kV), and the lamp starts to light up. The pulse continues until the lamp turns on (for about 1 to 2s.). But if the lamp does not turn on, the OFF output is developed. Q702 goes off after the lamp turned on, the igniter circuit stops the operation, and the DC50 to 70V is applied to the lamp.

SECTION III
OPTICAL SYSTEM

1. CONFIGURATION

	No.	Name	Description
Lamp unit	17	Metal halide lamp	Light source of the optical system. DC system,250W, short arc length 3mm. To use light effectively in the tilt projection system, the light axis is arranged to face upward.
	16	Elliptical reflector	Elliptical reflector converges light emitted from the metal halide-lamp, thereby creating light beams parallel with light axis and illuminating the beams to the liquid crystal panel.
	15	Capacitor lens	Converges the parallel light beams from the reflector in direction of focal point and effectively transmits the beams through 1.3 inch liquid crystal panel.
Mirror box unit	14, 12	Multi-lens	Multi-lens allows a circular beam light emitted from the light source to illuminate the square liquid crystal panel evenly, thus providing projected pictures with less brightness variation.
	13	Cold mirror	Visible light reflects at plane of incidence and goes to liquid crystal direction but infrared light and ultraviolet light penetrate, thus preventing undesired harmful light components from entering the liquid crystal panel.
	10a~ 10f	Dichroic mirror	Only red light component of white light emitted from the lamp transmits through 10a and reflected by 10b, and enters liquid crystal panel (R). At the same time, only green of green and blue light components reflected is reflected by 10c and enters G-panel. While the blue light component transmits through and enters B-panel. Light transmitted through each liquid crystal synthesized by the dichroic mirror 10f.
	5	Field lens	Light transmitted through liquid crystal panel is converged in direction of focal point and effectively entered entrance pupil of the projection lens.
	4	Phase difference plate/ incidence side polarized plate	Spectral characteristics for the dichroic mirror depend on polarization directions of the light (P-polarization, S-polarization). To use the characteristics, a place the phase difference plate which possesses the characteristics to rotate the polarization direction of light by 45 degrees is provided. When the spectral characteristic of S-polarization is important, the phase of S-polarization is converted so that it matches the transmission axis of the incidence side polarization plate for the S-polarization light to pass the panel best. On the other hand for the P-polarization, the phase is adjusted so that the P-polarization light passes the panel best. In this unit, when the S-polarization characteristic takes effective for the G-light component and when the P-polarization characteristic takes effective for the R and B light components, thus improving the light transmission amount projected from the optical unit and the color reproduction characteristics.
	3R 3G 3B	Liquid crystal panel (LCD)	Light exit side polarized plate and phase difference plate are put on the light exit plane. Polarization direction of transmission light rotates by 90 degrees when no signal voltage is applied, but a polarized plate has a characteristic which suppresses the rotation when a voltage is applied, To effectively use this characteristic, polarized plates, phase difference of polarized components transmitted through incidence side and exit side of which is 90 degrees, are located. That is, picture is displayed so that light transmits through most (white) when no signal voltage is applied and the light transmits through least (black) when a signal voltage is applied. Polarized light components transmitted through incidence side polarized plate is rotated by 45 degrees from Y axis in clockwise. This is to match aligning film of the liquid crystal panel for increasing efficiency of the light transmission. Phase difference plate rotates the exit side polarized plate by 45 degrees in counterclockwise direction (that is, in the light polarizing direction of the transmitting light) to obtain S-polarization light. This operation is to increase effect of polarized screen because, generally speaking, transmission axis of polarized screen has the same direction as that of S-polarization.
Projection lens	1	Projection lens	Projects pictures displayed on the liquid crystal at a wall, screen, etc. Light axis of the projection lens is located at upper side of center of the liquid crystal panel because of a tilt projection system employed. In a normal projection system, the projection screen is positioned at right angle to the unit. In this case, the unit body will disturb for persons to see the screen in practice. So, the projection will be directed upward, and this causes a trapezoidal distortion in the picture. To prevent this, the tilt projection system which allows the users to see the pictures projected without the trapezoidal distortion. (Figs. 3-4 and 3-5)



No.	Part name
1	Projection lens
3R	Liquid crystal panel (red)
3G	Liquid crystal panel (green)
3B	Liquid crystal panel (blue)
4	Phase difference plate + polarized plate
5	Field lens
9	Mirror box unit
10a-f	Dichroic mirror
12	Multi-lens B
13	Cold mirror
14	Multi-lens A
15	Capacitor lens
16	Elliptical reflector
17	Metal halide lamp
18	Lamp unit
19	High voltage supply

Fig. 3-1 Optical path diagram

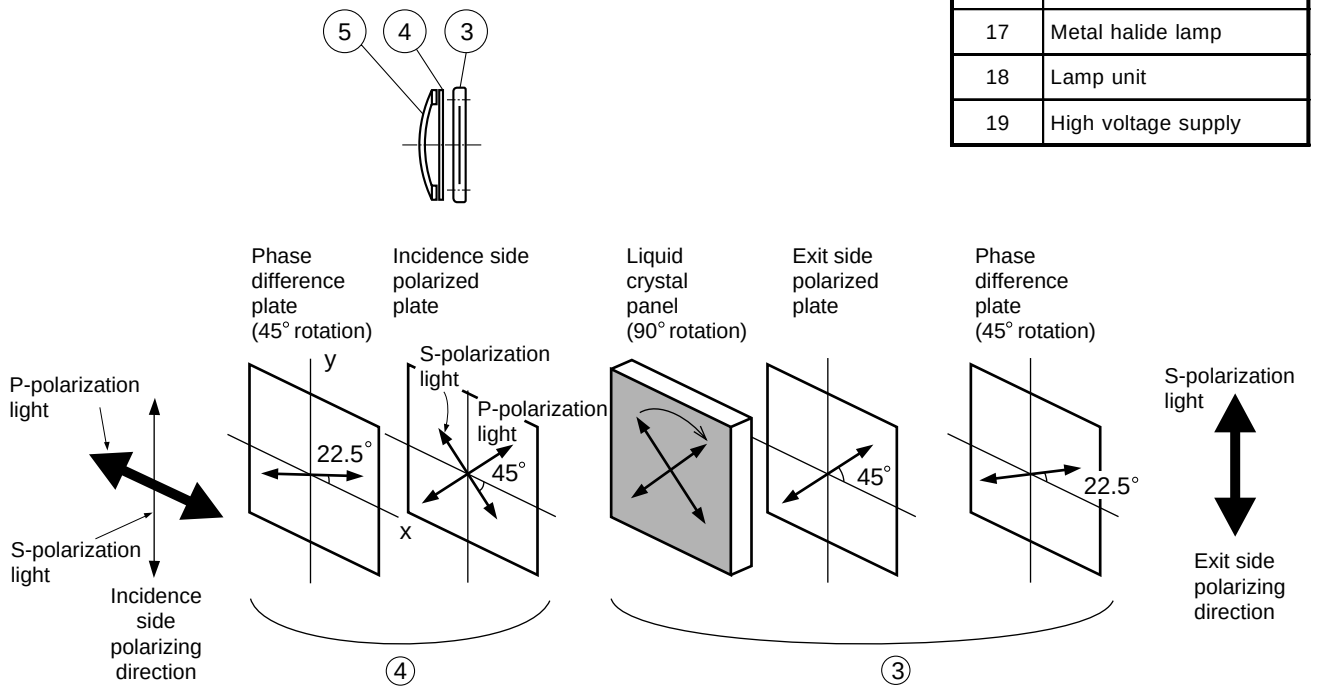


Fig. 3-2 Polarizing direction at each part (G light components)

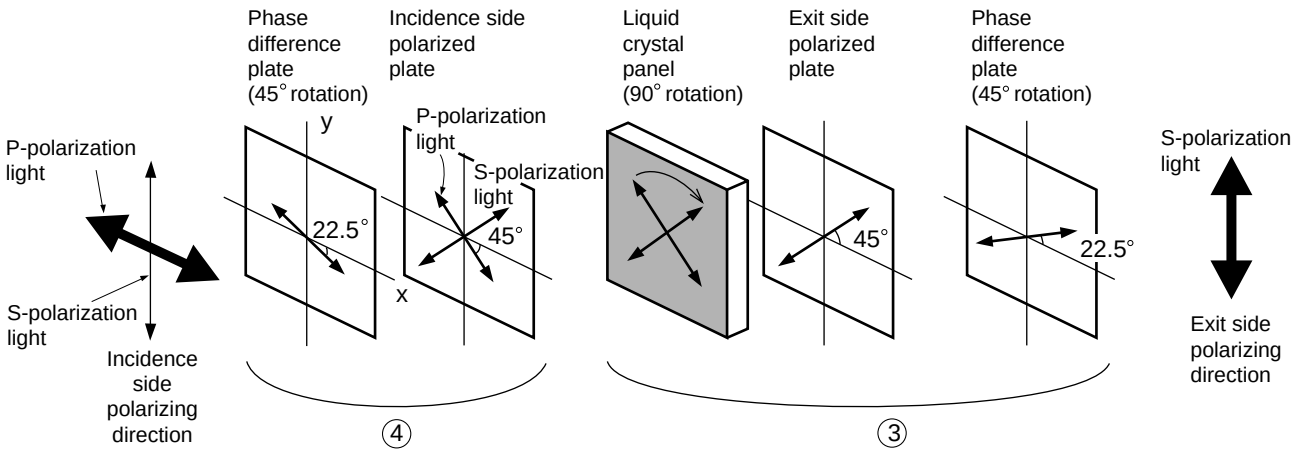
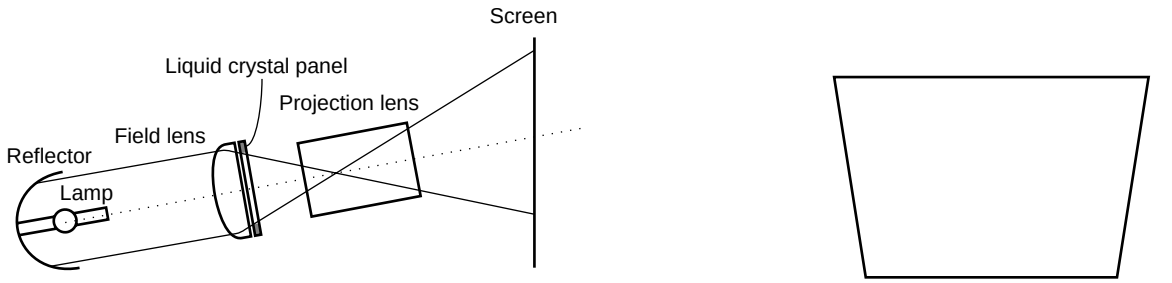
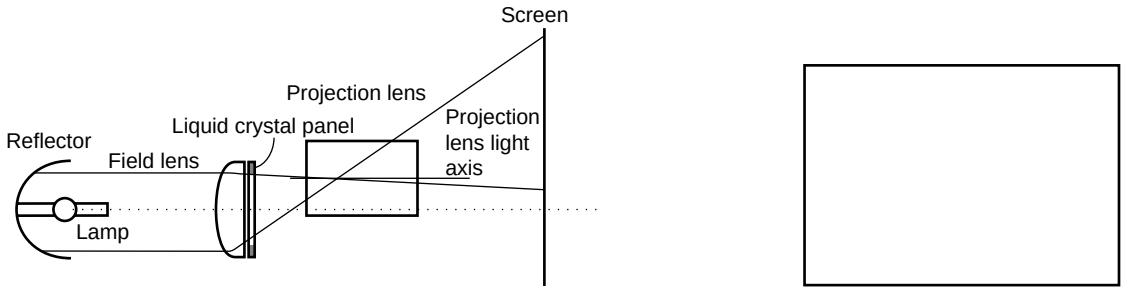


Fig. 3-3 Polarizing direction at each part (R/B light component)



(a) General projection system **(b) Picture by general projection system**

Fig. 3-4 General projection system



(a) Tilt projection system **(b) Picture by tilt projection system**

Fig. 3-5 Tilt projection system

SECTION IV
RGB DRIVE CIRCUIT

1. OUTLINE

This circuit is described using G process as an example and composed of level shifter, gamma (g), black limiter, inverted signal amplifier, sample & hold circuit and liquid crystal panel.

A block diagram of the drive circuit is shown in Fig. 4-1.

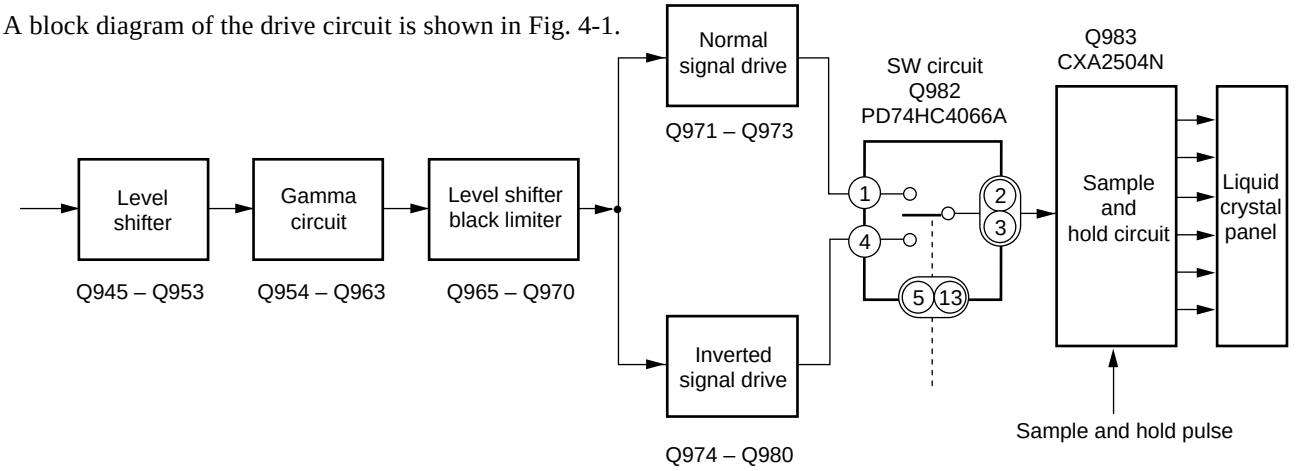


Fig. 4-1

2. CIRCUIT DESCRIPTION

The following description will be given assuming that V_{BE} of transistor is 0.7V.

2-1. Level Shifter (Q945 – Q953)

This circuit is composed of the emitter follower Q945, full feedback unit gain amplifier Q946 – Q950, and the current source circuit of sub bright for Q951 – Q953. The circuit operates to vary only the DC level of the input signal and develops the signal with only the DC level shifted from the input signal at Q949. The shift level is determined by the current flowing into R976.

When a triangular waveform of 2.3V – 3.6V shown in Fig. 4-2 is input, a triangular waveform of 3.0 – 4.3V appears at the base of Q946. At the same time, a triangular waveform of approx. 3.0V – 4.3V also appears at the base of Q948.

Assuming the sub brightness adjustment voltage at Q953 is 1.83 V_{DC}, a current of (1.83V – 0.7V)/(220 + 15) = 4.97 mA flows into Q951 and Q950, and this current also flows into R976. Therefore, the emitter voltage of Q949 develops 1.06V higher than the base voltage of Q948 as shown in the equation; 4.8 mA x 220W = 1.06V. And the triangular waveform of 4.06V – 5.36V appears at the emitter of Q949.

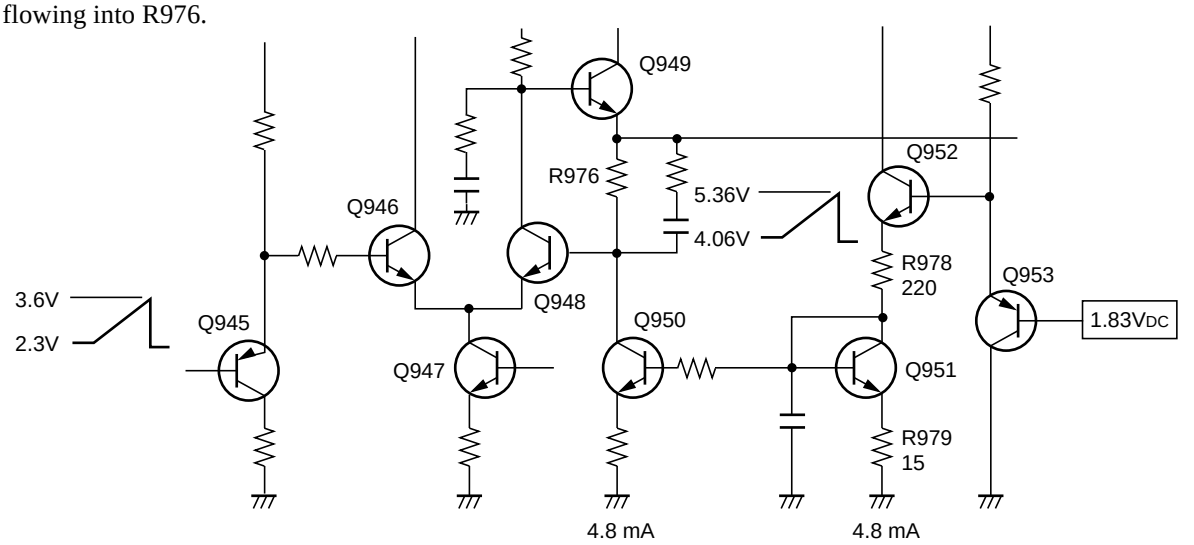


Fig. 4-2 Level shifter circuit

2-2. Gamma (g) Circuit

The circuit consists of a current source consisting of R983, R984, Q954, full feedback amplifier Q955 – Q960, the gain variation circuit Q961 – Q963 and R991. (The circuit including Q955 – Q963 is called the gamma circuit.)

A current of (12.7V – 0.7V)/(1.3 kW + 15W) = 9.15 mA is flown into the current source for Q954 and the same current is also flown into Q956 (Q947). At the same time, a current of 9.15 mA x (15/20) = 6.9 mA is flown into Q960.

The followings are described referring to Fig. 4-3.

The signal from the level shifter is supplied to the base of Q955. If the device elements and currents of Q955 and Q957 are exactly the same, the base state of Q955 is same as that of Q957. However, Q955 and Q957 are not paired in their characteristics, the actual base state will be different. The base state of Q957 is described by referring to the triangular waveform of 4.06V – 5.36V.

When the base of Q963 develops 3.55 V_{DC}, the emitter of Q961 develops 4.25 V_{DC}. In the signal area where the base of Q963 is higher than 4.25V, the current of 7.7 mA is flown into R988 because of Q961 turned off, and the emitter voltage of Q956 increases by amount of 1.7V, 7.7 mA x 220W = 1.7V, from the base of Q957. As the base voltage of Q957 is close to 4.25V, Q961 turns on and the current is flown into the collector of Q960 through R991.

When the base voltage of Q957 develops 4.06V, the current flowing into R991 is 2.8 mA, (4.25V – 4.06V)/68 = 2.8 mA. The current flowing into R998 decreases by that amount and the voltage shifting amount also decreases by the same amount, 2.8 mA x 220W = 0.62V. The operation is shown in Fig. 4-4.

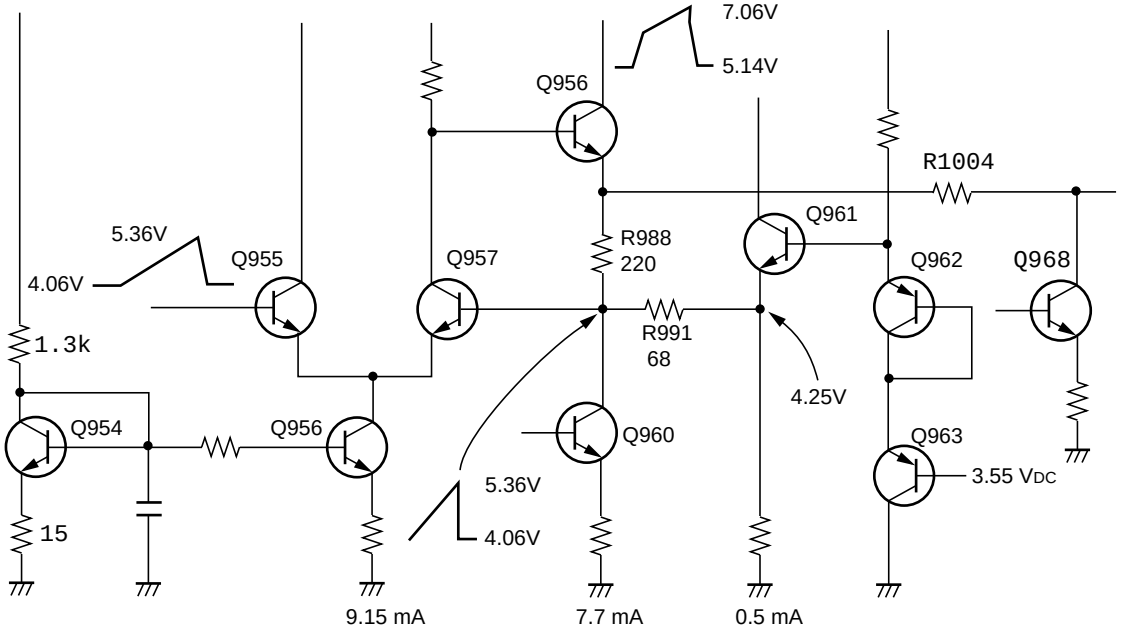


Fig. 4-3 Gamma circuit

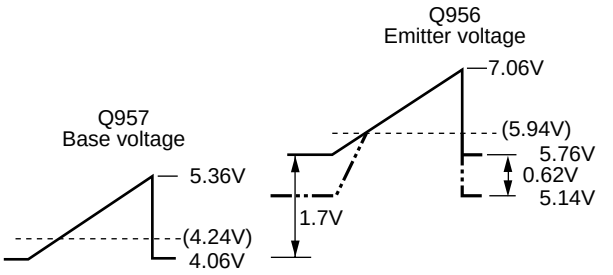


Fig. 4-4 Gamma circuit operation

2-3. Level Shifter Circuit (Q965 – Q968, R1044)

Q965 – Q967 works as a current source. Assuming that the base voltage of Q965 is 1.76 V_{DC}, the current 4.2 mA is flown into Q967 and the same current also flown into Q968. The current and R1044 make a voltage drop and only the DC level is shifted.

2-4. Black Limiter (Q969, Q970)

The black limiter is a switching circuit and its operation is as follows. When the base voltage of Q969 is higher than that of Q970, Q969 turns on and when the base voltage of Q969 is lower than that of Q970, Q969 turns off and Q970 turns on.

2-5. Inverted Signal Amplifiers (Q974 – Q981)

- Q974, Q975: Emitter follower
- Q976 – Q978: Inverted signal amplifier
- Q979 – Q981: Emitter follower

The op. amplifier is composed of Q976 – Q978. Q977 base accepts an inverted input and Q978 normal input. For easy understanding of the op. amplifier, an op. amplifier shown in Fig. 4-5 will be refferred.

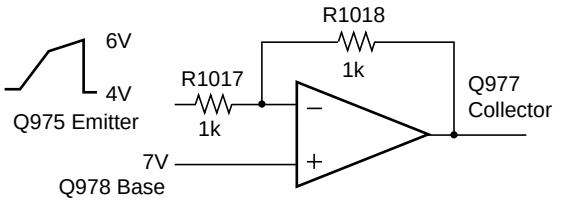


Fig. 4-5

The output of Q977 is 7V x (1 + R1018/R1017) – 4V = 10V, so 7V x (1 + R1018/R1017) – 6V = 8V is output. (The constant of R1017 is assumed to 1 kW, in considering the internal emitter resistor of Q975.)

Accordingly, the output shown in Fig. 4-6 is obtained.

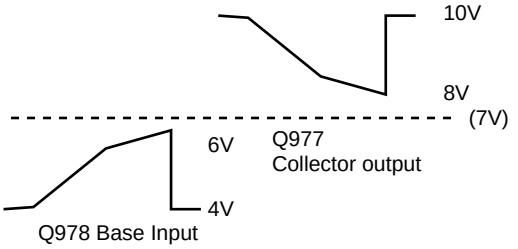


Fig. 4-6 Reverse output operation

2-6. Switch Circuit (Q982 µPD74HC4066A)

The normal and inverted signal outputs are switched for every horizontal and vertical period.

The signal is inverted for one horizontal period and then further inverted for one vertical period.

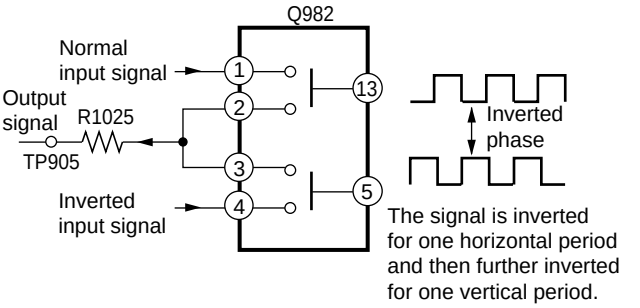


Fig. 4-7 SW circuit operation

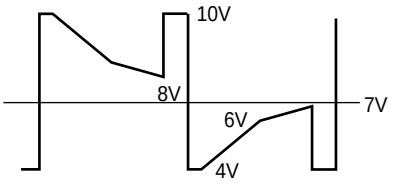


Fig. 4-8

2-7. Sample & Hold Circuit

The block diagram of the circuit is shown in Fig. 4-10 and its connection diagram is shown in Fig. 4-11. As shown in the block diagram in Fig. 4-9, 6CH, each consisting of the level shifter, S/H (sample and hold) and driver circuits, are contained in CXA2504N.

Each sample & hold operation is carried out on pins 18, 19, 20, 1, 2 & 3 and the re-sample & hold operations for 6CH are carried out together on pins 21 and 40. This means that the serial data is converted to the parallel data and the LCD panel operation frequency is lowered.

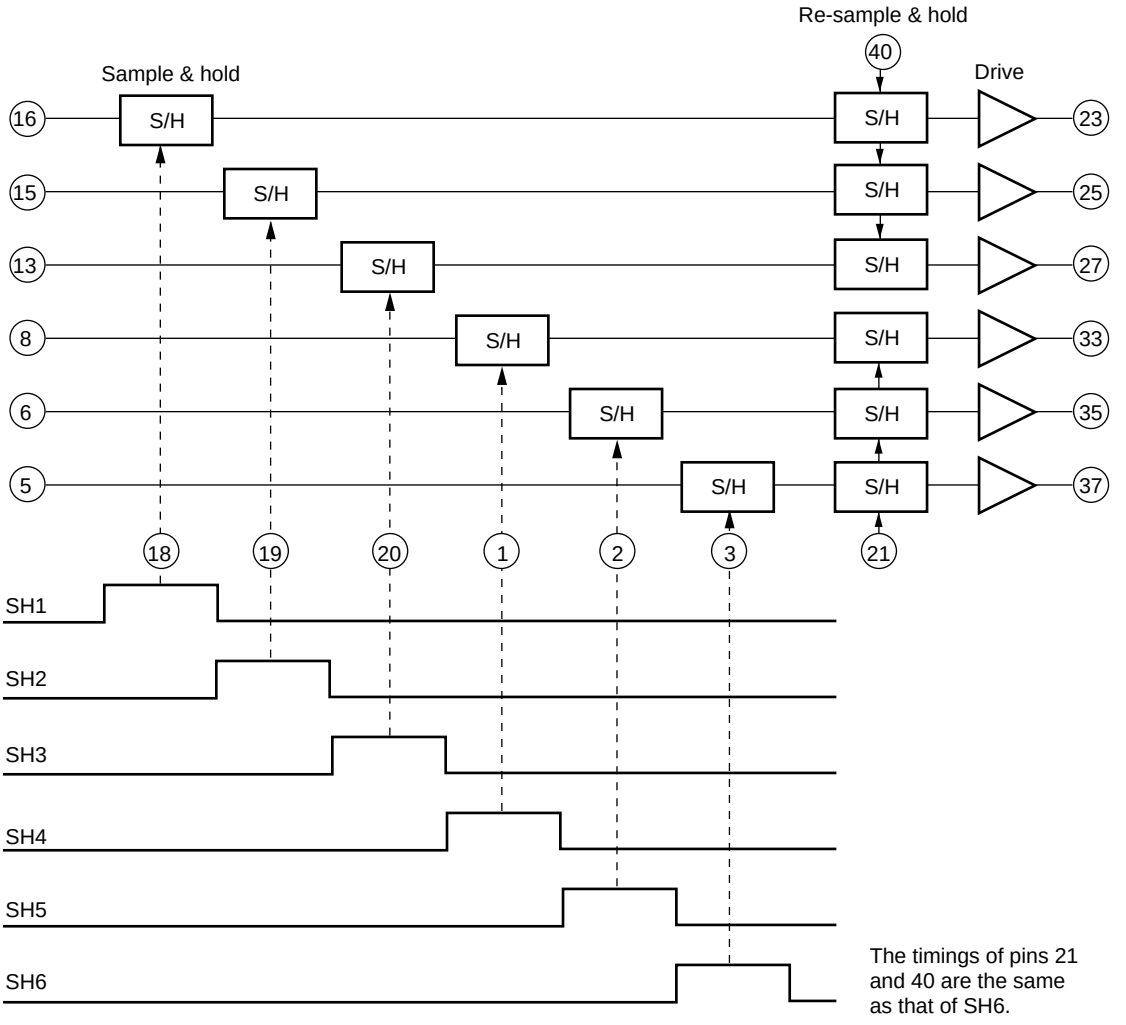


Fig. 4-9 Sample & hold operation

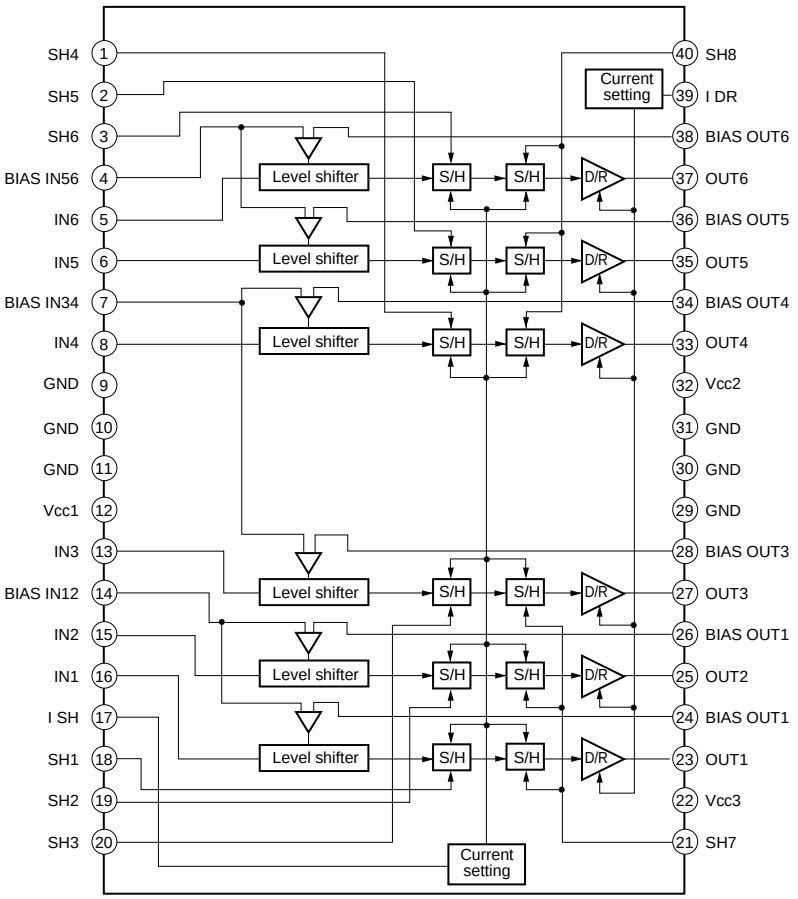


Fig. 4-10 CXA2504N block diagram

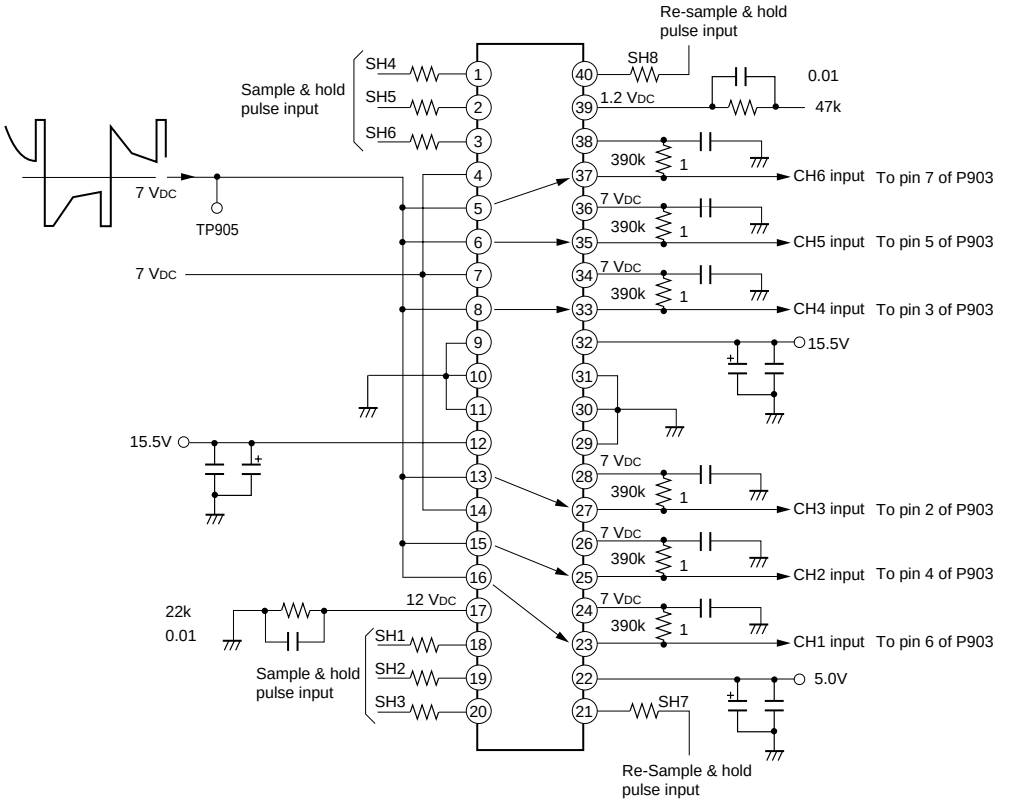


Fig. 4-11 Peripheral circuit of sample & hold circuit

2-8. LCD Panel

The LCD panel uses the active matrix panel with 3.3 cm in diagonal length and a built in driver made of the super thin film multi-crystal silicone transistor. Use of 3 panels enables to display in full color mode. The pixels are arranged in square form which is adequate for the data projection use. This realizes to display figures and characters clearly.

Also, use of a high luminance screen employing the advanced on-chip black matrix and a built-in cross-talk free circuit provides a high screen quality with less cross-talk.

The poly-silicone TFT high speed scanner is used and up/down and left/right inversion function is provided. Furthermore, use of 5V system interface circuit realizes a low voltage consumption for the timing and control signals.

2-8-1. Features

- Number of dots displayed: 519,000 dots in diagonal length of 3.3 cm (1.3 type)
- High transparent ratio: 20%
- Built-in cross-talk free circuit
- High contrast ratio in normally white mode: 200 (Standard)
- Built-in H, V driver (Built-in input level conversion circuit, 5V driving possible)
- Up/down and left/right inversion display function

2-8-2. Element component

- Number of dots: 832 (H) x 624 (V) = 519,168
- Active matrix panel with the driver using multi-crystal silicone transistors

The block diagram of the LCD panel is shown in Fig. 4-12 and terminal description is in Table 4-1.

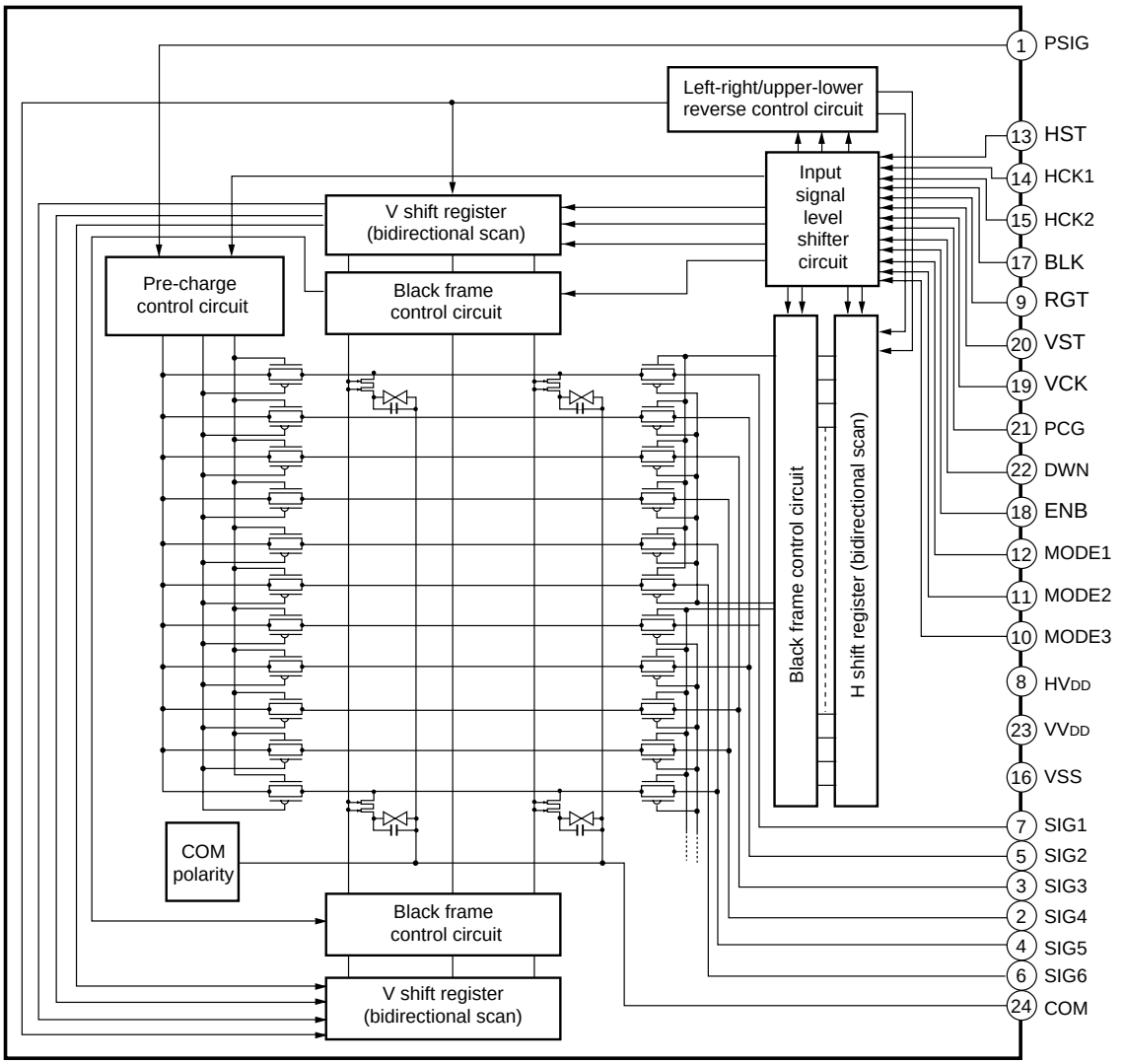


Fig. 4-12 Liquid crystal panel block diagram

The liquid crystal panel is provided with a built in display area variable circuit inside the liquid crystal panel. It is possible to correspond with each signal of MAC16/SVGA/VGA/PC98/NTSC/WIDE/PAL. The mode switching described above is carried out owing to the signal developed at pins 10 to 12 of the display area switch input terminal as shown in Fig. 4-13. The area not displayed (shaded portions in Fig. 4-13) is written by PSIG signal of pin 1.

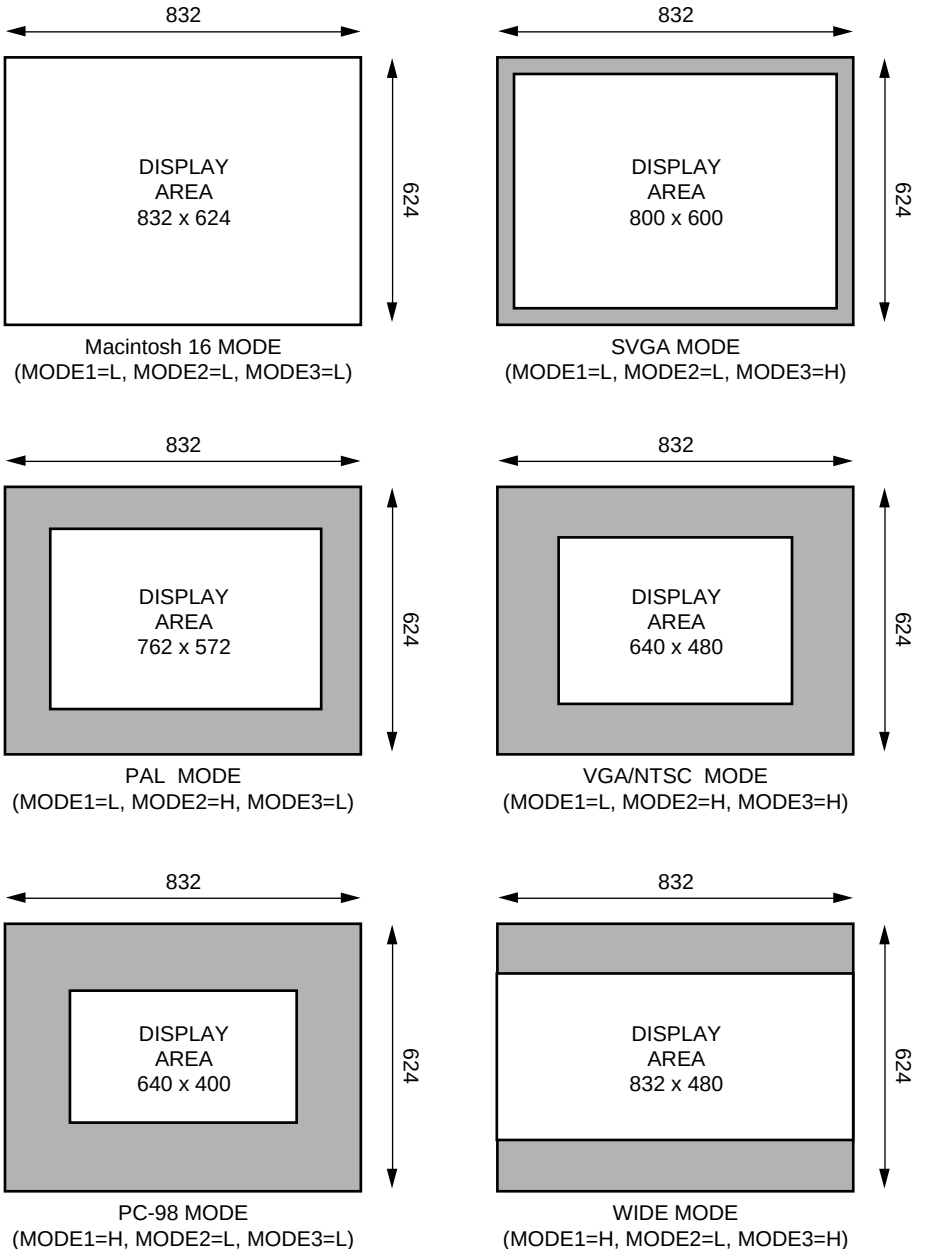
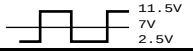


Fig. 4-13

Table 4-1 Liquid crystal panel terminal description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	PSIG	Uniformity improvement signal input terminal 	13	HST	Start pulse input terminal for H shift resistor driving
2	SIG4	Video signal 4 input terminal to LCD panel, 7V center ± 4.5 V max.	14	HCK1	Clock input terminal for H shift resistor driving
3	SIG3	Video signal 3 input terminal to LCD panel	15	HCK2	Clock input terminal for H shift resistor driving
4	SIG5	Video signal 5 input terminal to LCD panel	16	V_{SS}	GND terminal for H, V drivers, GND
5	SIG2	Video signal 2 input terminal to LCD panel	17	BLK	External frame display pulse input terminal
6	SIG6	Video signal 6 input terminal to LCD panel	18	ENB	Enable input terminal for gate selection pulse
7	SIG1	Video signal 1 input terminal to LCD panel	19	VCK	Clock input terminal for V shift resistor driving
8	HV_{DD}	Power supply input terminal for H driver, 15.5V	20	VST	Start pulse input terminal for V shift resistor driving
9	RGT	Driving direction input terminal for H shift resistor (H: Normal direction, L: Reverse direction)	21	PCG	Uniformity improvement pulse input terminal
10	MODE3	Display area SW 3 input terminal	22	DWN	Driving direction input terminal for V shift resist or (H: Normal direction, L: Reverse direction)
11	MODE2	Display area SW 2 input terminal	23	VV_{DD}	Power supply input terminal for V driver, 15.5V
12	MODE1	Display area SW 1 input terminal	24	COM	Counter power supply voltage input terminal for LCD panel, 6.6 V_{DC}

SECTION V
MICROCOMPUTER

1. SYSTEM OUTLINE

The system microcomputer has features as shown below.

In considering easy maintenance for specification modification, etc. an external program ROM is employed. The program is also developed in considering use of structured notation, parts modularity, and multi filling system.

Major functions of the system microcomputer are as follows.

(1) System control
- Power reset process
- Nonvolatile memory control process
- Remote control reception process
- RS-232C transmission and reception process
- Status reading process
- On-screen display process

(2) Normal control
- Power ON/OFF
- Input switch
- Sound volume control UP/DOWN
- Menu UP/DOWN
- Mute ON/OFF
- Display ON/OFF
- Adjusting value reset
- Focus UP/DOWN
- Zoom UP/DOWN

(3) Adjustment control
- Video controls (high & low brightness ratio, brightness, color density, tint, sharpness)
- Panel adjustments (V position, H position, phase, clock)
- Projection adjustments (Front projection, front projection with ceiling mount, rear projection, rear projection with ceiling mount)
- Mode adjustments (Enlarge, wide, OSD mute, user fixing)
- Adjustment data saving process
- Adjustment data default setting

(4) Adjustment control at shipping
- Video sub adjustments (RGB gain)
- Drive adjustments (each item)

Fig. 5-1 shows the system block diagram.

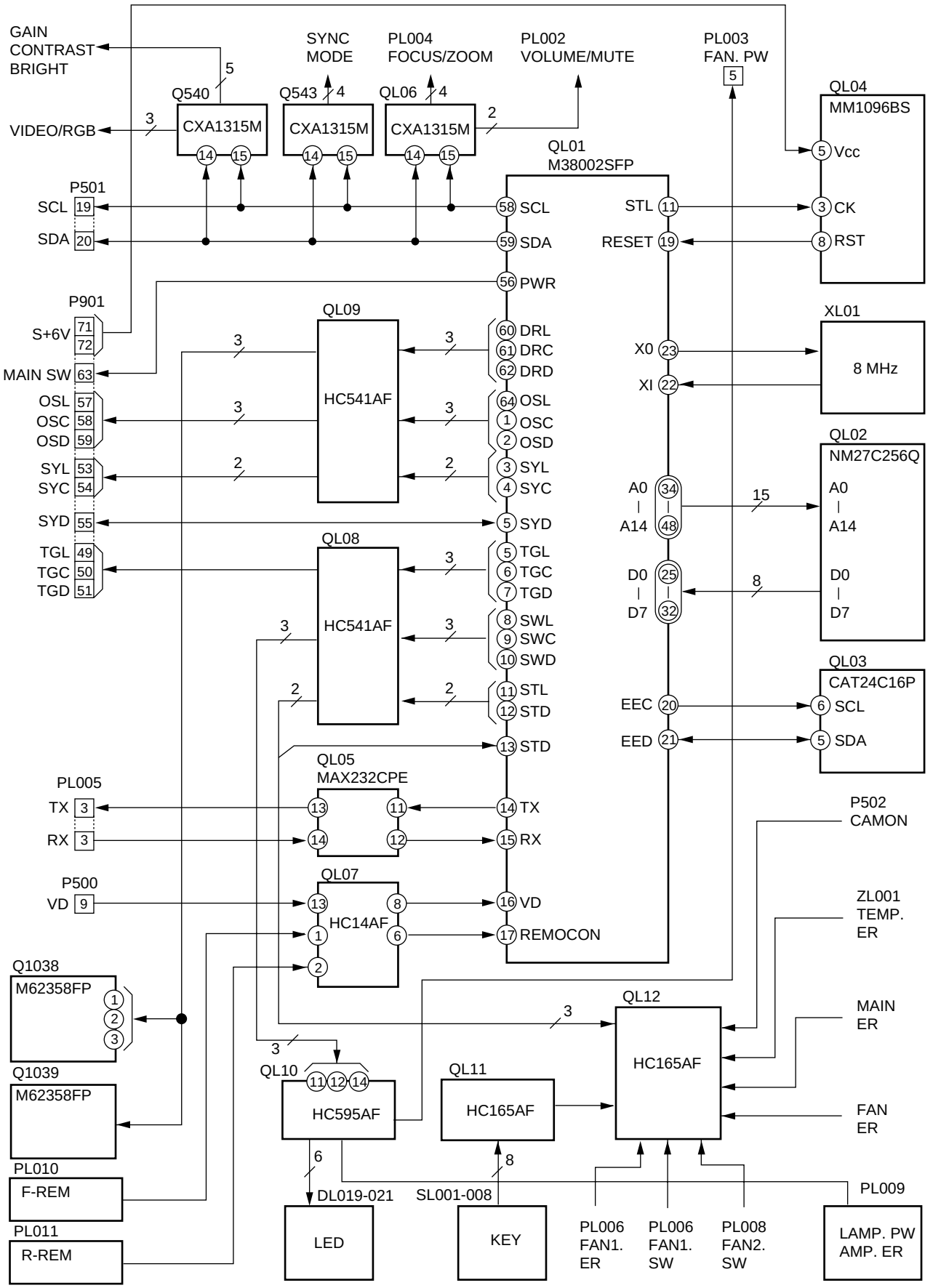


Fig. 5-1 System block diagram

2. SYSTEM MICROCOMPUTER

The system microcomputer QL01 employs an 8 bit microcontroller (M38002SFP).

In this system microcomputer, a program area provided inside the computer is not used but an external program ROM (QL02, NM27C256Q) is used.

This allows easy maintenance of the system when specification modification, bug correction, etc. will occur.

Table 5-1 shows the terminal function of the system microcomputer.

Table 5-1 Terminal function of the system microcomputer

Pin No.	Name	Function	I/O	Pin No.	Name	Function	I/O
1	OSD	UPD6453 clock	O	33	A15	Address for external ROM	O
2	SYL	SYG load	O	34	A14	Address for external ROM	O
3	SYC	SYG clock	O	35	A13	Address for external ROM	O
4	SYD	SYG data	I/O	36	A12	Address for external ROM	O
5	TGL	CXD2442 load	O	37	A11	Address for external ROM	O
6	TGC	CXD2442 clock	O	38	A10	Address for external ROM	O
7	TGD	CXD2442 data	O	39	A9	Address for external ROM	O
8	SWL	HC595 latch	O	40	A8	Address for external ROM	O
9	SWC	HC595 clock	O	41	A7	Address for external ROM	O
10	SWD	HC595 data	O	42	A6	Address for external ROM	O
11	STL	HC165 load	O	43	A5	Address for external ROM	O
12	STC	HC165 clock	O	44	A4	Address for external ROM	O
13	STD	HC165 data	I	45	A3	Address for external ROM	O
14	TX	RS-232C transmission data	O	46	A2	Address for external ROM	O
15	RX	RS-232C reception data	I	47	A1	Address for external ROM	O
16	VD	Vertical flyback period pulse	I	48	A0	Address for external ROM	O
17	RMC	Remote controller reception data	I	49			N. C
18	CNV_{SS}	Operation mode setting	I	50			N. C
19	RESET	External reset input	I	51			N. C
20	EEC	CAT241C16 clock	O	52			N. C
21	EED	CAT241C16 data	I/O	53			N. C
22	XI	OSC input	I	54	ONW	External weight	+5V
23	X0	OSC output	O	55			N. C
24	GND	GND (0V)	I	56	PWR	Power switch	O
25	D7	Data for external ROM	I	57	V_{CC}	Power supply (+5V)	I
26	D6	Data for external ROM	I	58	SCL	I^2C clock	O
27	D5	Data for external ROM	I	59	SDA	I^2C data	I/O
28	D4	Data for external ROM	I	60	DRL	M62358 load	O
29	D3	Data for external ROM	I	61	DRC	M62358 clock	O
30	D2	Data for external ROM	I	62	DRD	M62358 data	O
31	D1	Data for external ROM	I	63	OSL	UPD6453 load	O
32	D0	Data for external ROM	I	64	OSC	UPD6453 clock	O

3. POWER SUPPLY RESET PROCESS

In the power supply reset process, a watch dog timer (MM1096BS) is used as a power supply reset IC (QL04) as shown in Fig. 5-1.

The reset IC (QL04) accepts a clock pulse signal for the watch dog timer which is sent from WDT terminal of the microcomputer, determines the microcomputer is in an abnormal status due to some reason if the clock signal does not exist for about 1s , and sends a reset signal to the RESET terminal of the system microcomputer (QL01).

Fig. 5-2 shows the MN1096BS reset timing diagram.

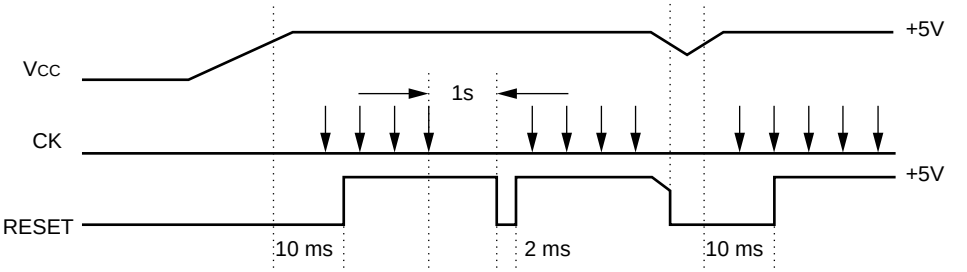


Fig. 5-2 MM1096BS reset timing diagram

4. NON-VOLATILE MEMORY PROCESS

In the non-volatile memory process, data reading and writing for various adjustments are carried out on the non-volatile memory (QL03: CAT24C16) as shown in Fig. 5-1.

When the power (AC) is on, all the adjustment data are read out by the system microcomputer (QL01) at the timing shown in the read out timing diagram of Fig. 5-3 (A), thereby realizing the previous status.

When saving the data, all the adjustment data are written by the system microcomputer (QL01) at the timing shown in the timing diagram of Fig. 5-3 (B), thereby keeping the current status.

However, if a failure (such as power interruption due to lightening, etc.) occurs during the adjustment data writing, a data error may occur. If the data is determined as incorrect, the initial data memorized on the system microcomputer (QL01) is read out and stored on the non-volatile memory.

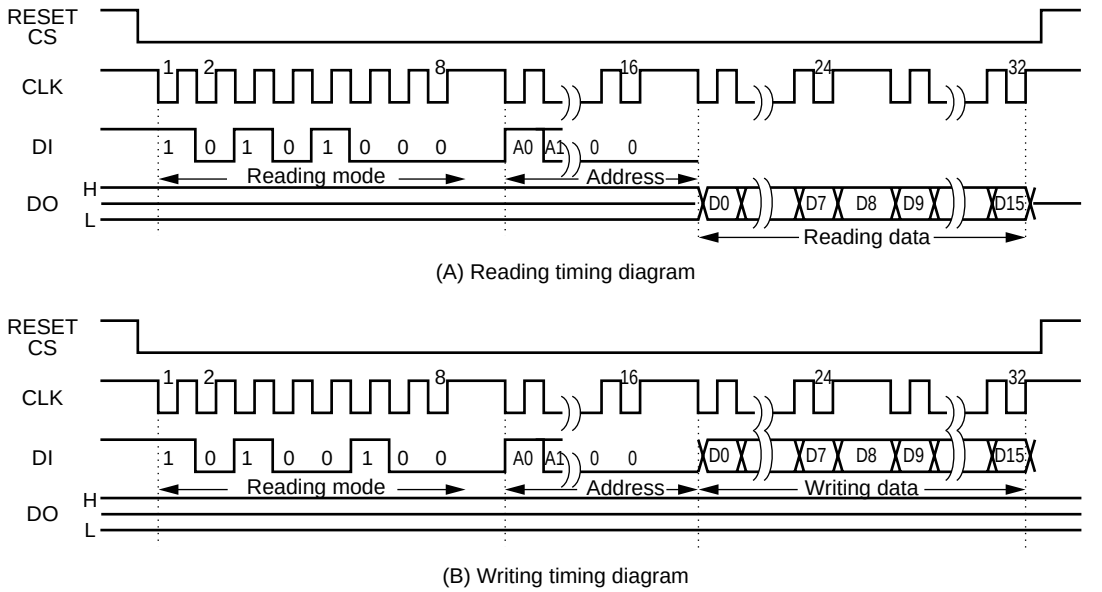


Fig. 5-3 Non-volatile memory timing diagram

5. REMOTE CONTROL RECEPTION PROCESS

In the remote control reception process, a remote control unit (CT-9888) connected to the remote control terminal emits a remote control signal and a remote control signal receive section (ZL002) on the front panel or a remote control signal receive section (ZL003) on the rear panel decodes the signal.

Each remote control signal decoded is mixed through the connectors of PL010 or PL011 and fed to the system microcomputer (QL01) through a buffer QL07 (MC74 HC14AF).

Fig. 5-4 shows the remote control signal reception timing diagram.

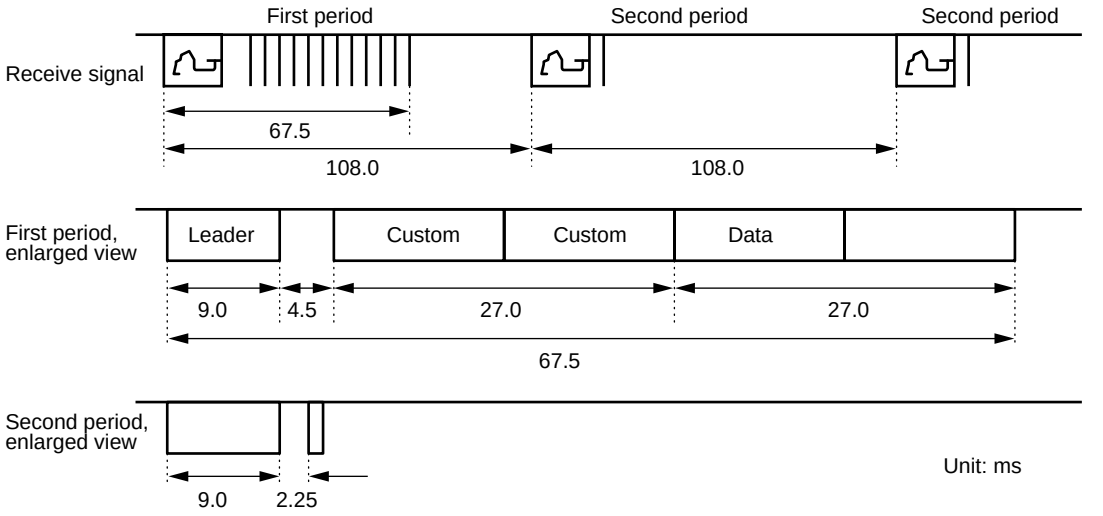


Fig. 5-4 Remote control signal reception timing diagram

6. RS-232C TRANSMIT/RECEIVE PROCESS

In the RS-232C transmit/receive process, an RS-232C signal entered through the RS-232C connector (D-SUB 9P) on the rear panel is decoded in the RS-232C interface (QL05: MAX232CPE), and fed to the system microcomputer (QL01) through PL005.

Fig. 5-5 shows the RS-232C signal timing diagram.

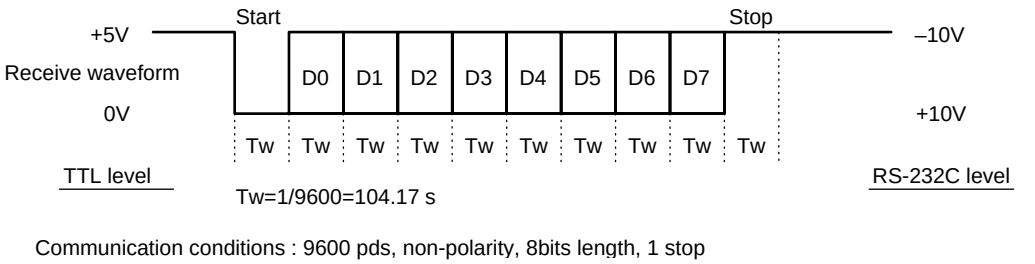


Fig. 5-5 RS-232C signal timing diagram

7. STATUS READ PROCESS

In the status read process, two data fetch ICs, QL11, QL12 (MC74HC165AF) as shown in Fig. 5-1, read the status.

Fig. 5-6 shows a data fetch timing diagram.

QL11 reads panel key status and QL12 does various status.

Table 5-2 shows the contents of the status read signals and the logic.

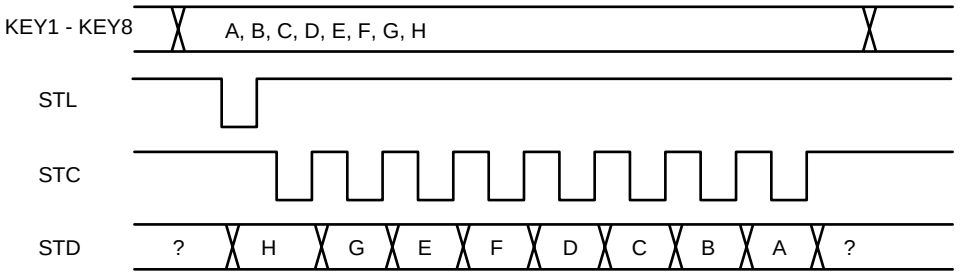


Fig. 5-6 Data fetch timing diagram

Table 5-2 Contents of the status read signals and the logic

Signal name	A	B	C	D	E	F	G	H
Pin No.	11	12	13	14	3	4	5	6
QL11	ON/ STANDBY	MENU (DOWN)	MENU (UP)	VOL/ADJ(-)	VOL/ADJ (+)	INPUT	AUX1	AUX2
(L)	ON	ON	ON	ON	ON	ON	ON	ON
(H)	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
QL12	FAN1. ER	FAN1. SW	FAN2. ER	MAIN. ER	LAMP. ER	FAN. ER	TEMP. ER	CAMON
(L)	Abnormal	Normal	Abnormal	Abnormal	Abnormal	Abnormal	Normal	Camera Yes
(H)	Normal	Abnormal	Normal	Normal	Normal	Normal	Abnormal	Camera Yes

8. STATUS DISPLAY PROCESS

In the status display process, a status display IC QL10 (MC74HC595AF) shown in Fig. 5-1 displays the status.

Fig. 5-7 shows the data display timing diagram.

Table 5-3 shows the contents of the status display signals and the logic.

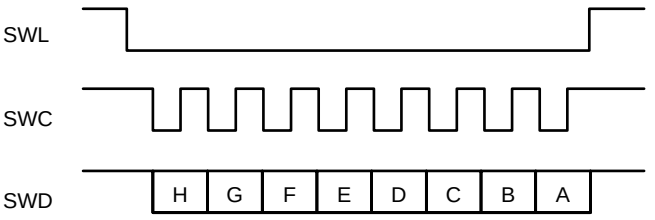


Fig. 5-7 Data display timing diagram

Table 5-3 Contents of the status display signals and the logic

Signal name	QA	QB	QC	QD	QE	QF	QG	QH
Pin No.	15	1	2	3	4	5	6	7
QL10	ON (red)	ON (green)	LAMP (red)	LAMP (green)	TEMP (red)	TEMP (green)	FAN. PW	LAMP. PW
(L)	LED off	LED off	LED off	LED off	LED off	LED off	OFF	OFF
(H)	LED on	LED on	LED on	LED on	LED on	LED on	ON	ON

9. ON-SCREEN DISPLAY PROCESS

In the on-screen display process, control signals are supplied to the OSD display IC QX43 (mPD6453) through P901, and the OSD display IC generates character display signals at the timing determined by VD, HD and clock supplied to the IC separately.

Fig. 5-8 shows the timing diagram for the on-screen control signals.

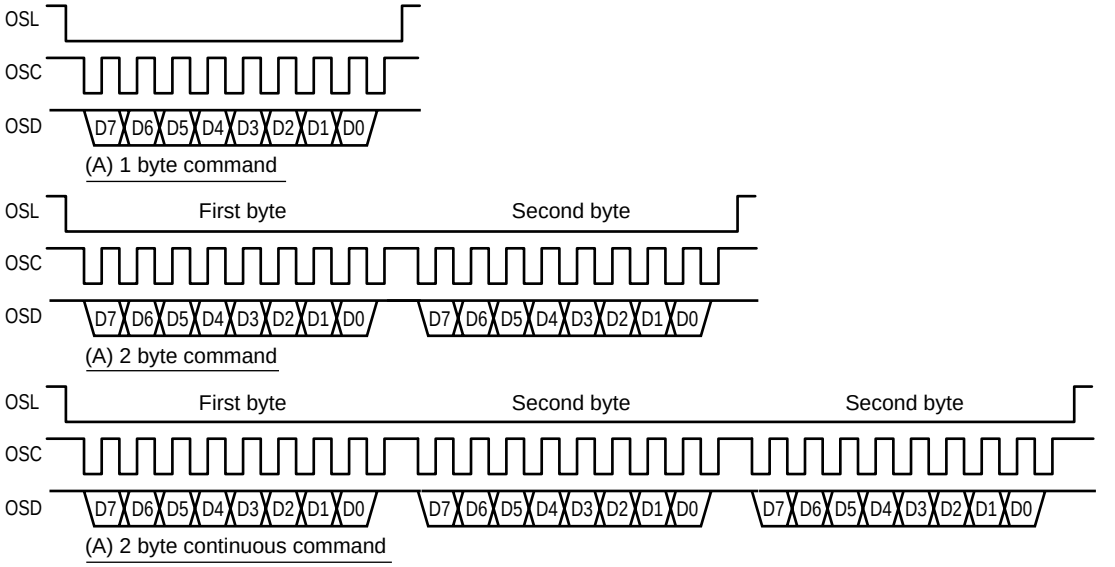


Fig. 5-8 Timing diagram for on-screen control signals

10. VIDEO MODE FETCH PROCESS

In the video mode fetch process, a status fetch IC Q543 (CXA1315M) fetches the status in the read mode of I^2C bus (Custom: $45).

Fig. 5-9 shows the I^2C bus read timing diagram. Table 5-4 shows the contents of the video mode signals and the logic.

Table 5-4
Contents of the video mode signals and the logic

Signal name	SW0	SW1	SW2	SW3
Pin No.	2	1	9	10
Q543	V. POL	H. POL	H. STATE	V. STATE
(L)	Positive polarity	Positive polarity	No	No
(H)	Negative polarity	Negative polarity	Yes	Yes

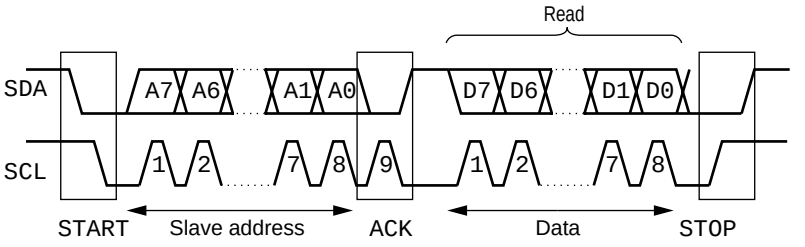


Fig. 5-9 I^2C bus read timing diagram

11. VIDEO SYSTEM CONTROL PROCESS

In the video system control process, control signals are supplied to various video system process ICs through P501.

Fig. 5-10 shows the I^2C bus timing diagram and table 5-5 shows the contents of process in each kind of IC.

Table 5-5 Contents of process in each kind of IC

Part No.	Type name	Contents of process
Q540	CXA1315M (Custom: $42)	Brightness, contrast, RGB gain, Video/RGB input switching
Q200	TA1218N (Custom: $90)	Input signal (Video/Audio), Video/S terminal input
Q201	TC9090N (Custom: $8A)	Color signal process (3D Y/C separation)
Q220	TDA9141 (Custom: $8A)	Sync detection process (Custom: $8B), Signal kinds identification (NTSC/PAL/SECAM, etc.)
Q223	TDA4780 (Custom: $88)	Video control (Color density, tint)
Q222	TDA4672 (Custom: $88)	Video control (Sharpness control)

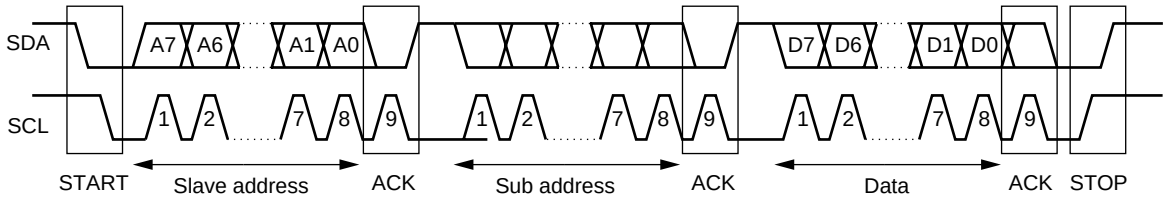


Fig. 5-10 I^2C bus timing diagram

12. PANEL SYSTEM CONTROL PROCESS

The panel system control process supplies various control signals to the panel system control ICs through P901.

Table 5-6 shows the contents of process in each kind of IC.

Fig. 5-11 shows the M62358FP control bus timing diagram, Fig. 5-12 does the CXD2442Q control bus timing diagram, Fig. 5-13 does the SYG read mode bus timing diagram and Fig. 5-14 does the SYG write mode bus timing diagram.

Table 5-6 Contents of process in each kind of IC

Part No.	Type name	Contents of process
Q1038 Q1039	M62358FP	Panel drive process
QX45	CXD2442Q	Screen position control (V position , H position , sample phase) Panel display control (Projection, attribution, etc.)
QX32	SYG (TC160G54F-113)	Screen process control process (sample frequency), Various screen display process (position, frame, attribution, etc.)

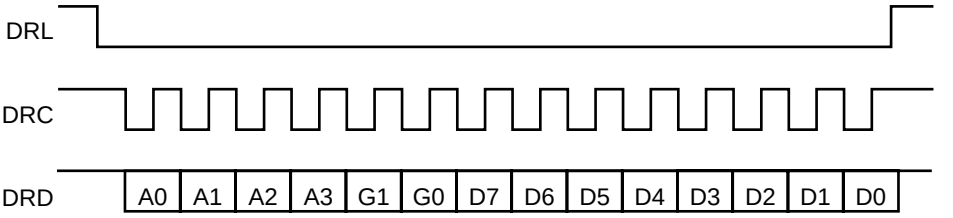


Fig. 5-11 M62358FP control bus timing diagram

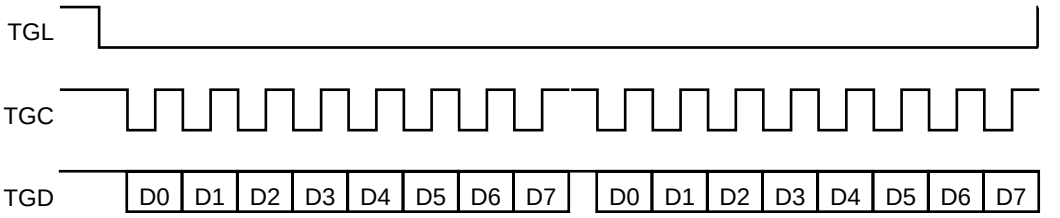


Fig. 5-12 CXD2442Q control bus timing diagram

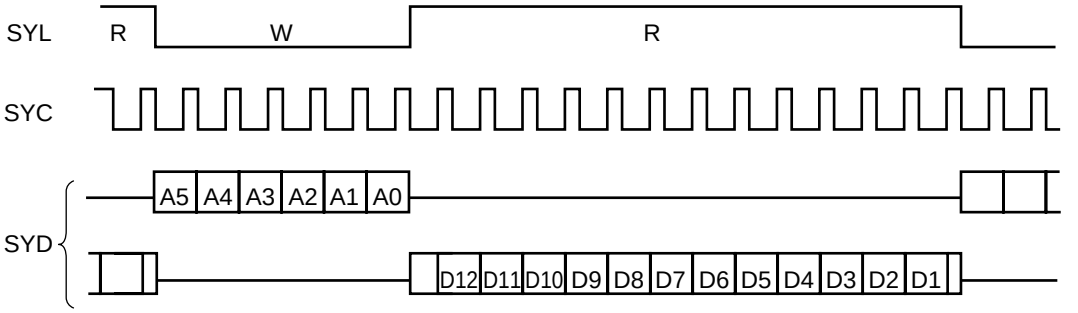


Fig. 5-13 SYG read mode bus timing diagram

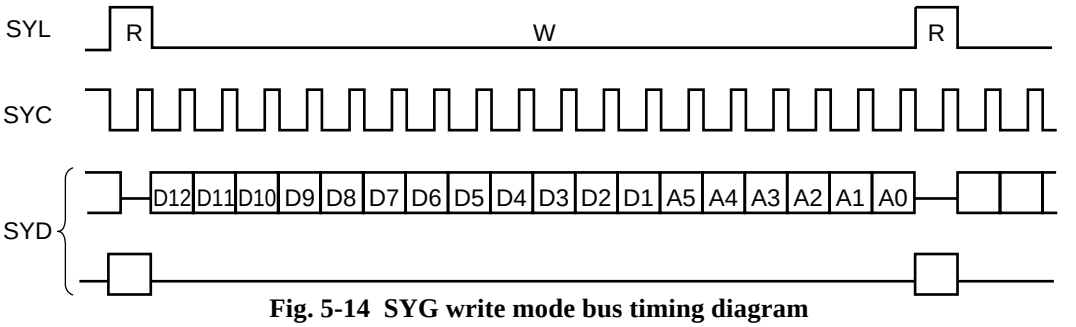


Fig. 5-14 SYG write mode bus timing diagram

13. VARIOUS DISPLAY MODES

In this system, various LED display patterns are provided in relation to the display modes shown in Table 5-7. Operations from AC on to power on and power off will be given below.

Data of the non-volatile memory are checked at the AC on, and all the LED are turned on in red in the initial use. In second or later use, all the LEDs are turned on in green and the unit enters the standby status.

In the standby status, only the STANDBY/ON LED is turned on in orange, and the main power is off and the lamp power is also off.

When the power is on by pressing the STANDBY/ON key, the unit enters a normal status in passing through following processes.

1. The main power is on, and STANDBY/ON LED turns on in green.
2. The lamp power is on, and LAMP LED blinks in green for about 3s.
3. With the lamp turned on, LAMP LED turns on in green and the unit enters the normal status.
4. If the lamp does not turn on, STANDBY/ON LED turns on in orange, and the LAMP LED blinks for about 1 min. and then the unit returns to the standby status.

In the normal status, STANDBY/ON LED and the LAMP LED are turned on in green, and the main power and the lamp power are turned on.

When the power is turned off by pressing the STANDBY/ON key, the unit enters the standby status in passing through following processes.

1. When the lamp power is turned off, STANDBY/ON LED turns on in orange.
2. The LAMP LED blinks in green for about 1 min. For this period the lamp can not be turned on again by the STANDBY/ON key.
3. When blinking of the LAMP LED stops, only the STANDBY/ON LED turns on in orange. After this the lamp can be turned on again by the STANDBY/ON key.
4. Moreover, the fan works for about 2 min. to lower temperature of the unit. For this period the main power is kept turning on.
5. When the main power turns off, the fan also stops and returns to the standby status.

If an error occurs due to some causes, the STANDBY/ON LED turns on in red, and the error information is kept in the display status of the LAMP and TEMP LEDs. When the error is detected, the unit enters the standby status after cooling down process for about 2 min. In this case, if the error status continues, the error display is also kept and any key entry is not accepted.

For the error due to the over time of the lamp-on time, the error is not released until the internal timer is reset (booting the system by turning the AC on with [–], [+], and [INPUT] keys pressed at the same time) after replacement of the lamp.

Table 5-7 Table of various display modes

ON	LAMP	TEMP	Contents	Status	Remedy
X	X	X	Standby power abnormal	at AC on	Repair
Green	Green	Green	Non-volatile memory OK	at AC on	Normal
Red	Red	Red	Non-volatile memory NG	at AC on	Initialization
Orange	X	X	Standby	at off	Normal
Green	X	X	Lamp on	at on	Normal
Green	(Green)	X	Lamp heat up	at on	Normal
Green	Green	X	Lamp on	during on	Normal
Green	X	X	Lamp off	at off	Normal
Orange	(Green)	X	Lamp cooling down	at off	Normal
Red	X	X	Main power abnormal	at/during on	Repair
Red	Red	X	Lamp not turns on	at/during on	Repair or preparation failure
Red	Orange	X	Lamp life terminated	at on	Works after about 2500H
Red	X	(Red)	Air suction fan stop	at on	Repair
Red	X	(Orange)	Exhaust fan stop	at on	Repair
Red	X	(Green)	Fan filter open	always	Close
Red	X	Red	Temperature sensor 1 abnormal	always	Lowers temperature inside unit

X stands for off, ( ) stands for blinking.

14. APPLICABLE SIGNAL

Quite a signals are used as the applicable signals in the preset mode (standard value) as shown in table 5-10. For the signals not fit to the preset modes, a user mode is provided.

In the preset modes, the applicable signals are based on the VESA standard, so the sample frequency (CLOCK adjustment in the panel menu) is not used, but the adjustment is allowed only in the user mode.

In the user mode, the signal line number is detected to allow the separate adjustment in the VGA system (basically effective for line number of 480/400/350 lines) and SVGA system (basically effective for line number of 600 lines).

In the user mode of SVGA system, the input signal is applicable to the plain display mode only in the XGA system (basically effective for line number of 768 lines) . That is, the signal is displayed.

Table 5-8 Applicable signal

Signal		Resolution		All		Frequency			Sync	Operation	
Mode	Content	H	V	H	V	H	V	Clock	H/V	Check	Remarks
NTSC	NTSC	664	484	800	525	15.730	59.940	12.590	N/N	O	Video input
PAL	PAL	756	574	800	625	15.630	50.000	12.500	N/N	O	Video input
V60	VGA 60 Hz	640	480	800	525	31.470	59.940	25.175	N/N	O	
V70	VGA 70 Hz	720	350	900	450	31.470	70.020	28.322	P/N	Δ	
V70	VGA 70 Hz	720	400	900	450	31.470	70.020	28.322	N/P	Δ	
V70	VGA 70 Hz	640	350	800	450	31.470	70.020	28.322	P/N	O	
V70	VGA 70 Hz	640	400	800	450	31.470	70.020	28.322	N/P	O	
V72	VGA 72 Hz	640	480	832	520	37.860	72.810	31.500	N/N	O	
V75	VGA 75 Hz	640	480	840	500	37.500	75.000	31.500	N/N	O	
V85	VGA 85 Hz	640	350	832	445	37.861	85.080	31.500	P/N	O	
V85	VGA 85 Hz	640	400	832	445	37.861	85.080	31.500	N/P	O	
V85	VGA 85 Hz	720	400	936	446	37.927	85.039	35.500	N/P	Δ	
V85	VGA 85 Hz	640	480	832	509	43.269	85.008	36.000	N/N	O	
M13	MAC-13"	640	480	864	525	35.000	66.670	30.240	N/N	O	
24K	PC98	640	400	848	444	24.830	56.420	21.053	N/N	O	
S56	SVGA 56 Hz	800	600	1024	625	35.160	56.250	36.000	N/N	O	
S60	SVGA 60 Hz	800	600	1056	628	37.880	60.320	40.000	N/N	O	
S72	SVGA 72 Hz	800	600	1040	666	48.080	72.190	50.000	N/N	O	
S75	SVGA 75 Hz	800	600	1056	625	46.880	75.000	49.500	N/N	O	
S85	SVGA 85 Hz	800	600	1048	631	53.674	85.061	56.250	N/N	O	
M16	MAC-16"	832	624	1152	667	49.720	74.550	57.283	N/N	O	
USHI	XGA 60 Hz	1024	768	1344	806	48.363	60.004	65.000	N/N	◆	Plain display
USHI	XGA 70 Hz	1024	768	1328	806	54.476	70.069	75.000	N/N	◆	Plain display
USHI	XGA 75 Hz	1024	768	1312	800	60.023	75.029	78.750	N/N	X	Plain display
USHI	XGA 85 Hz	1024	768	1376	808	68.677	84.997	94.500	N/N	X	Plain display

- In the sync column of table 5-8, P shows the positive polarity and N shows the negative polarity.
- In the operation column, O shows a standard mode, D shows pull-in mode, ¨ shows plain display mode and X shows the signal is out of correspondence.

15. RS-232C CONTROL METHOD

Signals are connected to the RS-232C connector in a straight format as shown in Table 5-9 RS-232C connection signals. This is because a crossing connection is provided inside the unit. Communication conditions are set to meet the conditions given in Table 5-10.

Table 5-9 RS-232C connection signals

Pin No.	Signal name	Signal content	I/O
2	RXD	Receive data	I
3	TXD	Transmit data	O
4	DTR	Data terminal ready	O
5	S. G	Signal ground	I
6	DSR	Data set ready	I
7	RTS	Transmission request	O
8	CTS	Transmission enable	I

Table 5-10 RS-232C communication conditions

Item	Conditions
Communication system	Transmission speed 9600 baud, No parity, data length 8 bit, Stop bit: 1 bit
Communication type	STX (1 byte) + CMD (3 byte) + ETX (1 byte) = 1 block STX is 02h, ETX is 03h, CMD is command string (Uppercase character)

16. RS-232C COMMAND LIST

Table 5-11 shows the RS-232C command list.

As a return value for a specified command received, an acknowledgment signal (ACK = 06h) is output when the command is correctly received within the operating conditions, or a non-acknowledgment signal (NAK = 16h) is output without the operating condition. Nothing is output if reception terminates abnormally.

When sending a command, leave the interval for at least 100 ms. Moreover, a longer process time is necessary at the power on or off, and input switching, so take care to leave a sufficient interval.

Table 5-11 RS-232C command list

Item	Display	Panel key	Remote control key	Command	Content
Power supply		STANDBY/ON	STANDBY/ON	PON	Power supply ON
		STANDBY/ON	STANDBY/ON	POF	Power supply OFF
Input switch		INPUT	INPUT	IN1	Video input
		INPUT	INPUT	IN2	RGBinput
		INPUT	INPUT	IN2	Camera input
Volume	VOLUME	VOL/ADJ +	VOL/ADJ +	VUP	Volume UP
		VOL/ADJ -	VOL/ADJ -	VDW	Volume DOWN
Adjustment		VOL/ADJ +	VOL/ADJ +	AUP	Adjustment value UP
		VOL/ADJ -	VOL/ADJ -	ADW	Adjustment value DOWN
Focus			FOCUS UP	FUP	Focus UP
			FOCUS DOWN	FDW	Focus DOWN
Zoom			FOCUS UP	ZUP	Zoom UP
			FOCUS DOWN	ZDW	Zoom DOWN
Menu		MENU UP/DOWN	MENU UP/DOWN		Menu UP/DOWN
Display			CALL	DON	Display ON
			CALL	DOF	Display OFF
Mute	MUTE		MUTE	MON	Mute ON
			MUTE	MOF	Mute OFF
Reset			RESET	RST	Standard setting for each item
Save	SAVE DATA	by menu	by menu	SAV	Adjustment value saving
Standard	PRESET DATA	by menu	by menu	PRE	Adjustment value standard setting
Contrast ratio	CONTRAST	by menu	by menu	VCN	Contrast
Brightness	BRIGHT	by menu	by menu	VBR	Brightness
Density	COLOR	by menu	by menu	VCL	Color
Hue	TINT	by menu	by menu	VTN	Tint
Picture quality	SHARP	by menu	by menu	VSH	Sharpness
V position	V-POS	by menu	by menu	SPV	Vertical position
H position	H-POS	by menu	by menu	SPH	Horizontal position
Sample phase	PHASE	by menu	by menu	SCP	Sample phase
Sample frequency	CLOCK	by menu	by menu	SCF	Sample frequency
Floor mounted front projection	STANDARD	by menu	by menu	PJ0	Floor mounted front projection
Ceiling mounted front projection	CEILING	by menu	by menu	PJ1	Ceiling mounted front projection
Floor mounted rear projection	REAR	by menu	by menu	PJ2	Floor mounted rear projection
Ceiling mounted rear projection	REAR CEILING	by menu	by menu	PJ3	Ceiling mounted rear projection

SECTION VI
DIGITAL CIRCUIT

1. DIGITAL CIRCUIT OPERATION

In the digital circuit, the following operations are carried out; video signal double speed conversion/enlargement process (NTSC signal), sync generation/Various kinds of timing signal generation necessary for liquid crystal panel driving and on-screen signal generation. Fig. 6-1 shows the digital circuit block diagram.

1-1. Display Mode

This unit uses a liquid crystal panel with 832 x 624 pixels. Basically, the effective pixel number (scanning line number) in the vertical direction is specified as the display pixel number in the vertical direction and the display pixel number in the horizontal direction is determined in relation to the aspect ratio of the signal system used.

Accordingly, The display area displayed on the panel differs owing to the input signal and the area not displayed is masked. The masked area is generated by writing the mode signal for the liquid crystal panel during the blanking period.

Accordingly, the signal supplied to the liquid crystal panel is a usual non-interlace signal and any blanking period is not added. For more details, refer to item 2-8 in section 4 (Page 4-7).

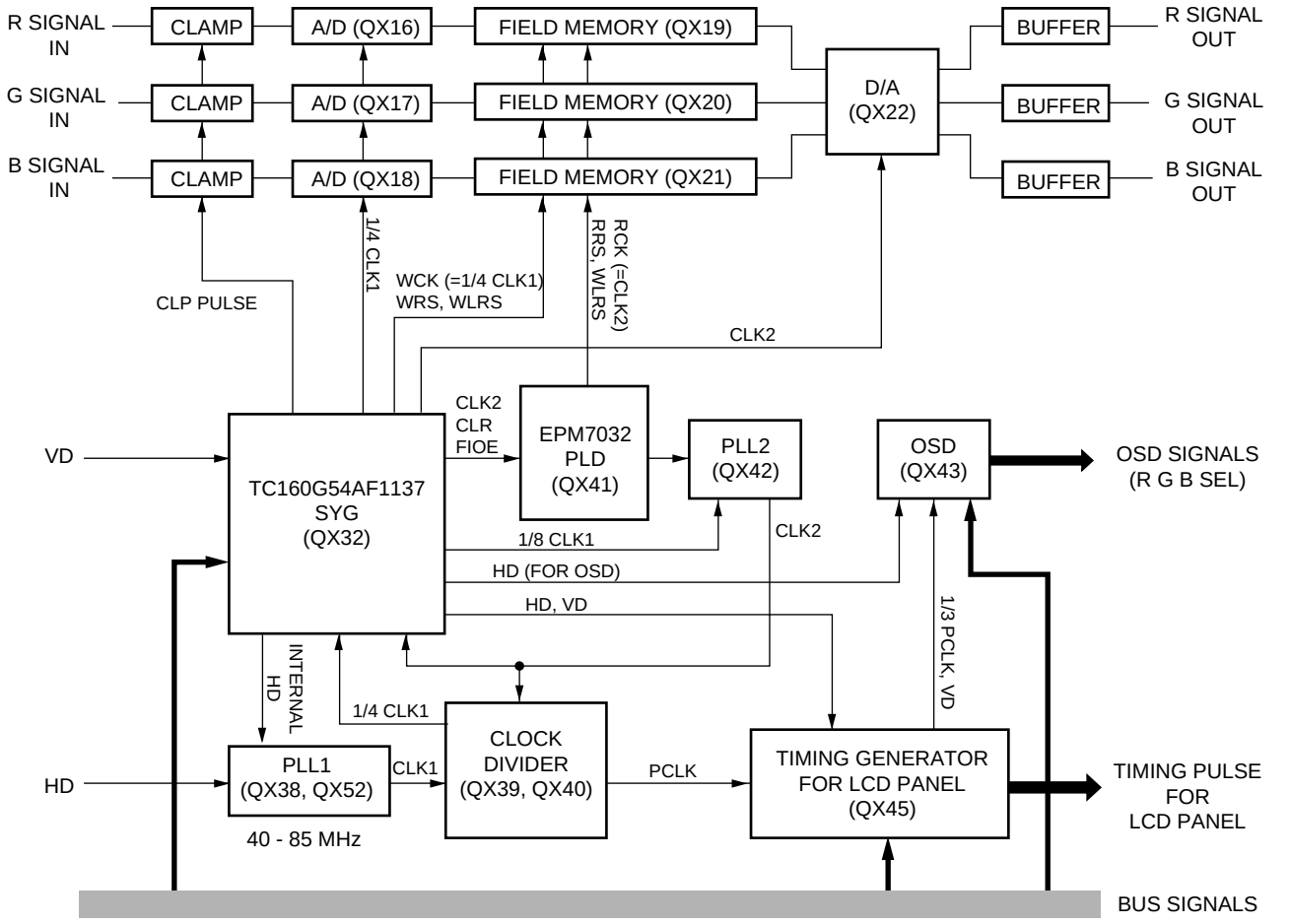


Fig. 6-1 Digital circuit block diagram

1-2. RGB Signal Input

When the RGB signals are input, sync generation, various kinds of timing signals generation for liquid crystal panel driving, and on-screen signal generation are carried out in the digital circuit. The video signal inputs to the RGB signal process circuit directly without passing through the digital circuit. So, each of the A/D converter, field memory and D/A converter circuit is operating actually, however, they are not used in practice. And, PLD and PLL circuit (2) stop their operation. These circuit are used when the video signal is input.

Fig. 6-2 shows the flow of timing signals when RGB signals are input. PCLK input to QX45 is a sampling clock as shown in Fig. 6-2. The oscillation range of the VCO composing of PLL (1) is 40 ~ 85 MHz, so the signal is divided in 1/2 in the clock divider circuit and used as a PCLK when a dot clock signal of 20 ~ 40 MHz (VGA system and SVGA@56 signal) is input. Further, 1/4 clock signal of VCO oscillation frequency is supplied to SYG (QX32), and operates SYG.

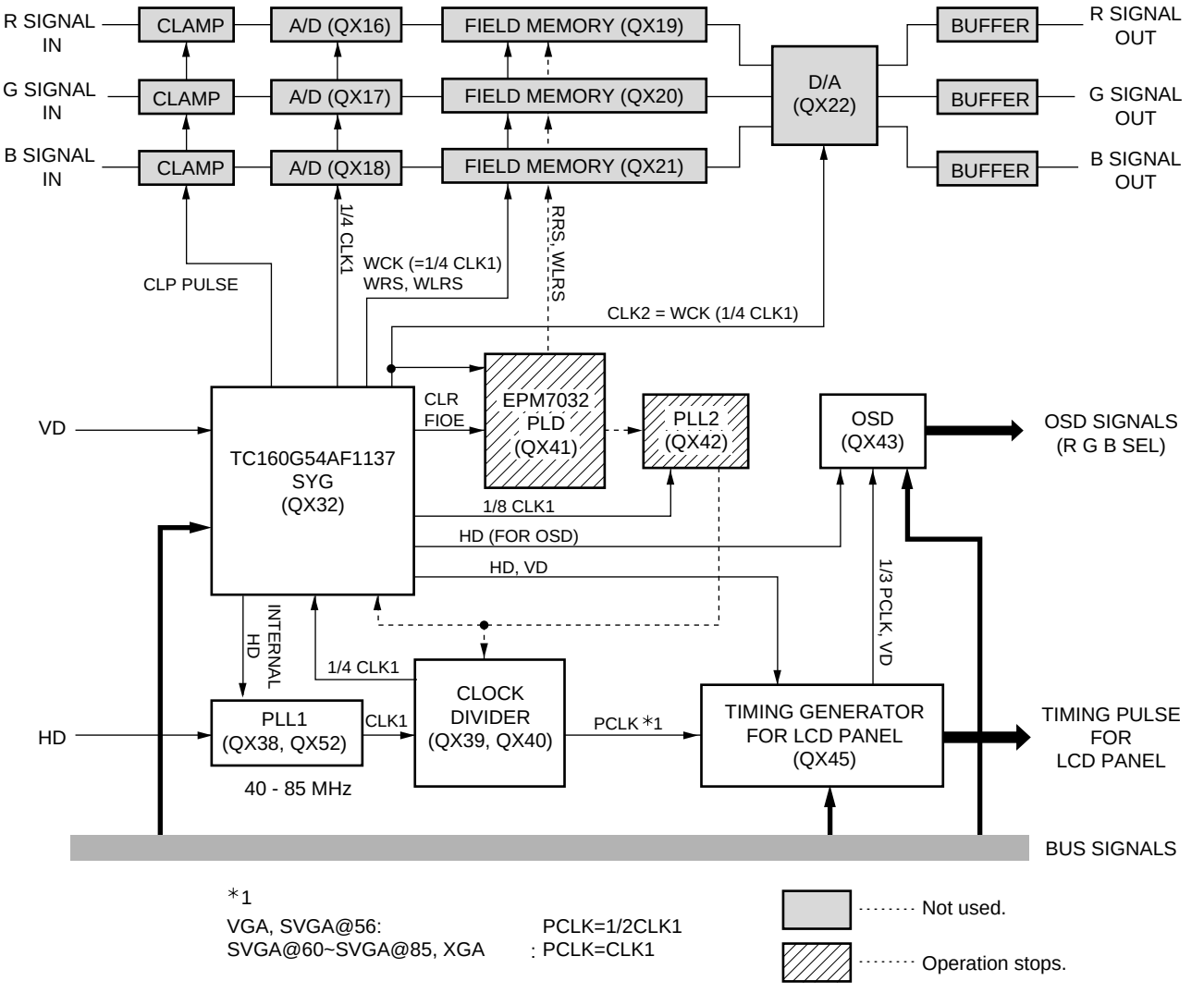


Fig. 6-2 Flow of timing signals when RGB signals are input

1-3. NTSC Signal Input

NTSC signal is operated in three modes; standard mode to display a picture with 640 x 480 pixels in the center area of the screen, enlargement mode to display a picture fully on the screen and WIDE mode (832 x 480) to display a picture fully in the horizontal direction.

Among three modes, in the standard and WIDE modes, the input signal is simply converted to a double speed signal. In the enlargement mode, the picture on the screen is enlarged 1.25 times in the vertical direction. This is realized by reading out one line twice and then three times alternately, though one line is read out two times usually. As for the precise circuit operation, refer to PLD description. The enlargement in the horizontal direction is carried out by changing the sampling number for one line.

In the standard mode, sampling operation is carried out by 832 fH = approx 12.8 MHz clock signal. In the enlargement mode, 1028 fH = approx. 16.2 MHz, and in WIDE mode, 1068 fH = approx. 16.8 MHz. The clock signal is generated in the PLL circuit (1).

In the PLL circuit (2), a clock signal for memory read is generated. In the standard mode, the clock signal generated is twice as much as the memory write clock signal (4-divided clock signal generated in the PLL (1)). And in the enlargement mode the clock signal generated is 2.5 times. Fig. 6-3 shows the operation when NTSC signal is input

1-4. PAL/SECAM Signal Input

The vertical effective line number for PAL signal is 575 lines and this displays a picture in 762 x 572 pixels area. When PAL signal is displayed the enlargement and WIDE modes are not available. The basic operation is the same as the NTSC signal standard mode. A clock signal generated in PLL (1) is activated with 942 fH = approx. 14.7 MHz and in PLL (2) it is activated with 29.4 MHz. The operation with the PAL signal is the same as shown in Fig. 6-3 (same as the NTSC standard mode.)

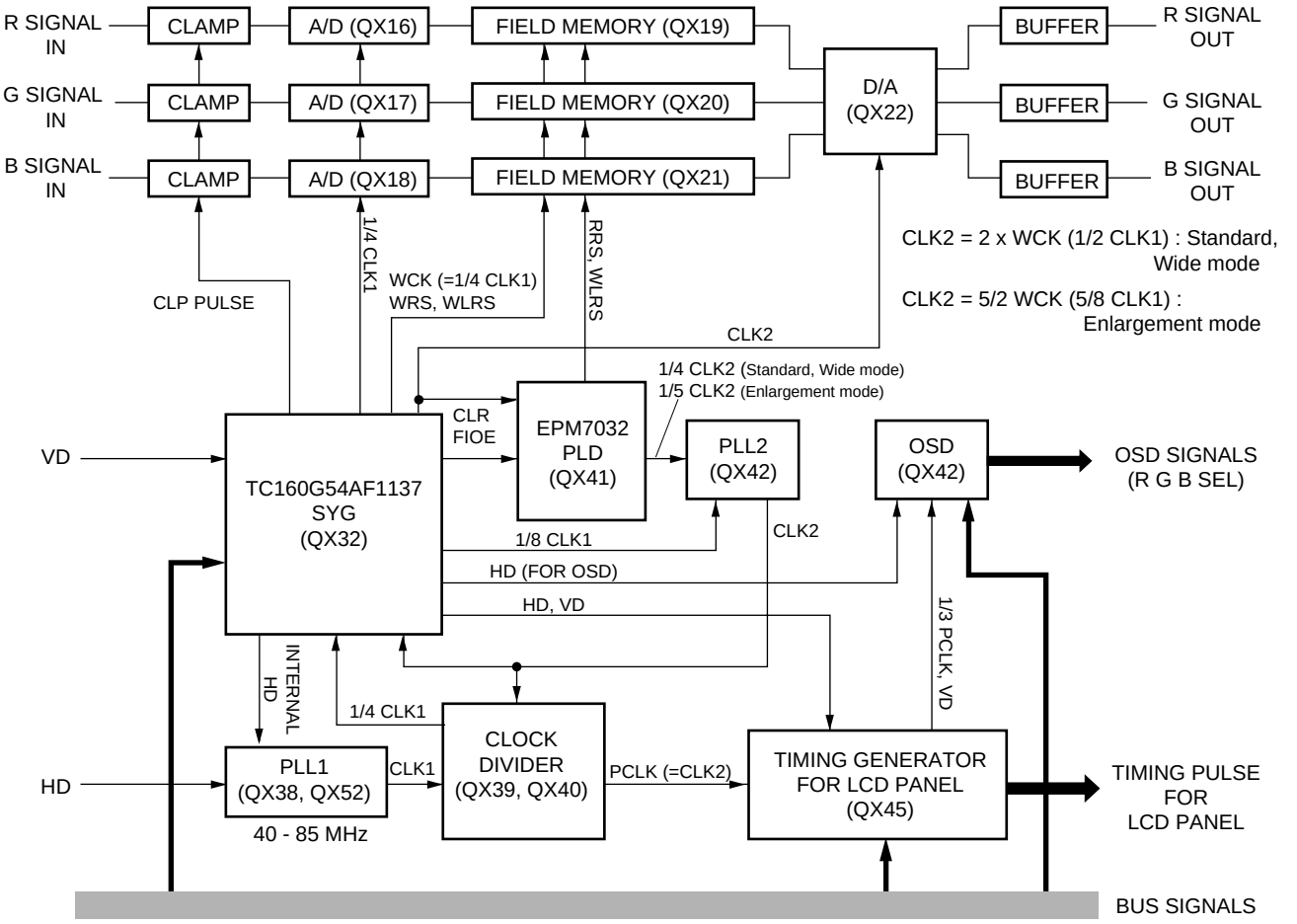


Fig. 6-3 Operation when Video signal is input

2. CIRCUIT DESCRIPTION

2-1. Clamp Circuit

A/D converter converts the video signal demodulated to RGB signals in the digital signals to perform digital-process.

The video signal is clamped to fit the reference level of the A/D converter. The clamp is of a pedestal clamp type and uses the reference level voltage of A/D converter. The actual clamp voltage potential is approx. 1.2V.

Fig. 6-4 shows the clamp circuit for G signal section.

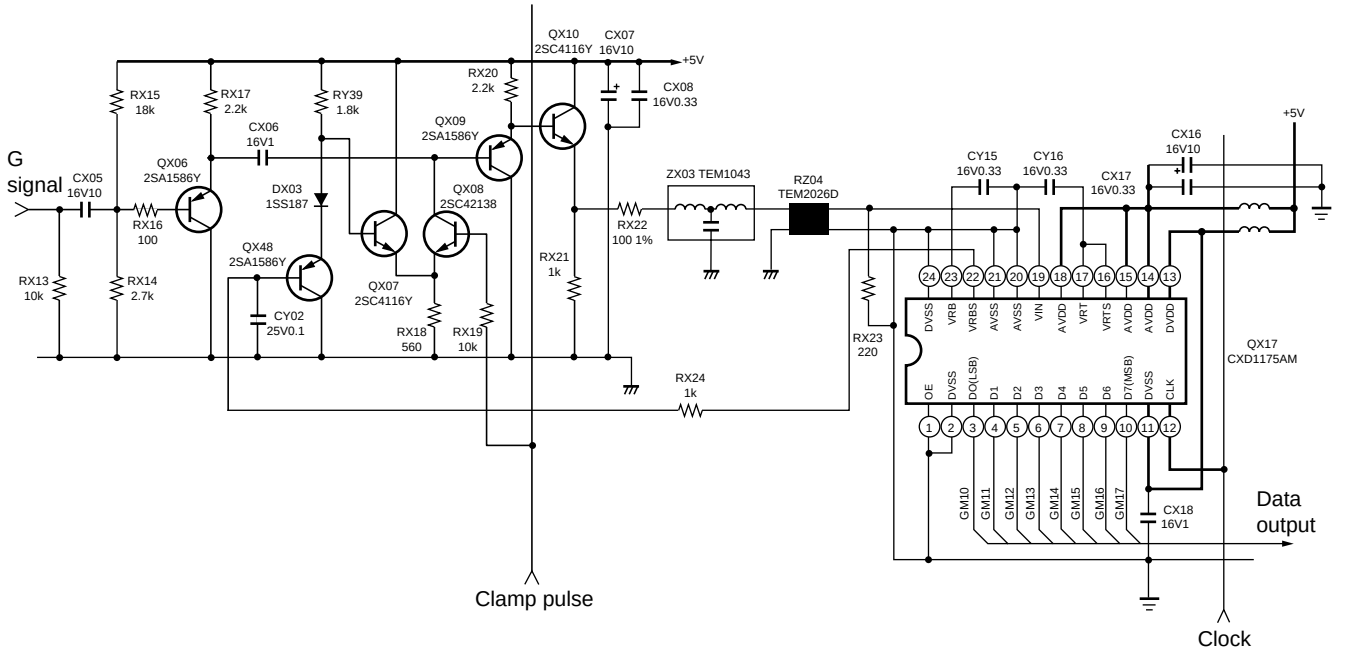


Fig. 6-4 Clamp circuit diagram

2-2. A/D Converter

Either CXD1175AM manufactured by SONY or TLC5510INS manufactured by TI is used for A/D converter (QX16, QX17 and QX18).

Both of CSD1175AM and TLC5510NS are equivalent and are 8-bits C-MOS A/D converter with maximum conversion rate of 20M sample/s.

Fig. 6-5 shows pin configuration of CXD1175AM and table 6-6 shows the terminal functions, and Fig. 6-6 shows the internal block diagram.

The signal input voltage range of the IC varies from 0.5 to 2.5V and the IC is used for each RGB channel. Totally three ICs are used.

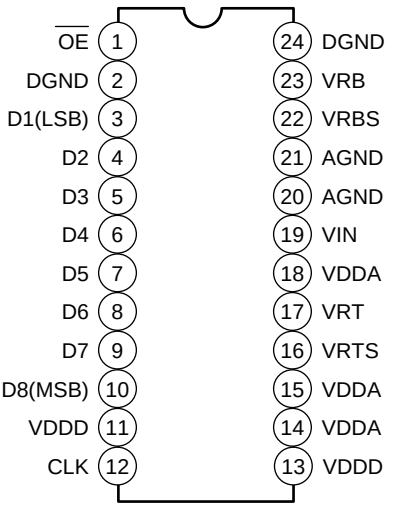


Fig. 6-5 Pin configuration of µPD6453GT

Table 6-1 CXD1175AM pin function

Pin No.	Name	Functions
1	$\overline{OE}$	Output enable terminal $\overline{OE}$ = "L" level: data enable $\overline{OE}$ = "H" level: output high impedance
2, 24	DGND	Digital GND terminal
3 - 10	D1 - D8	Data otput terminal D1: LSB, D8: MSB
11, 13	V_{DDD}	Digital power supply terminal
12	CLK	Clock input terminal
16	V_{RTS}	Reference voltage output terminal (upper) Short-circuit to V_{RT} when using internal reference voltage. Develops 2.63V.
17	V_{RT}	Reference voltage input terminal (upper)
23	V_{RB}	Reference voltage input terminal (lower)
14, 15, 18	V_{DDA}	Analog power supply
19	V_{IN}	Analog input terminal
20, 21	AGND	Analog GND terminal
22	V_{RBS}	Reference voltage output terminal (Lower) Short-circuit to V_{RB} when using internal reference voltage. Develops 0.61V.

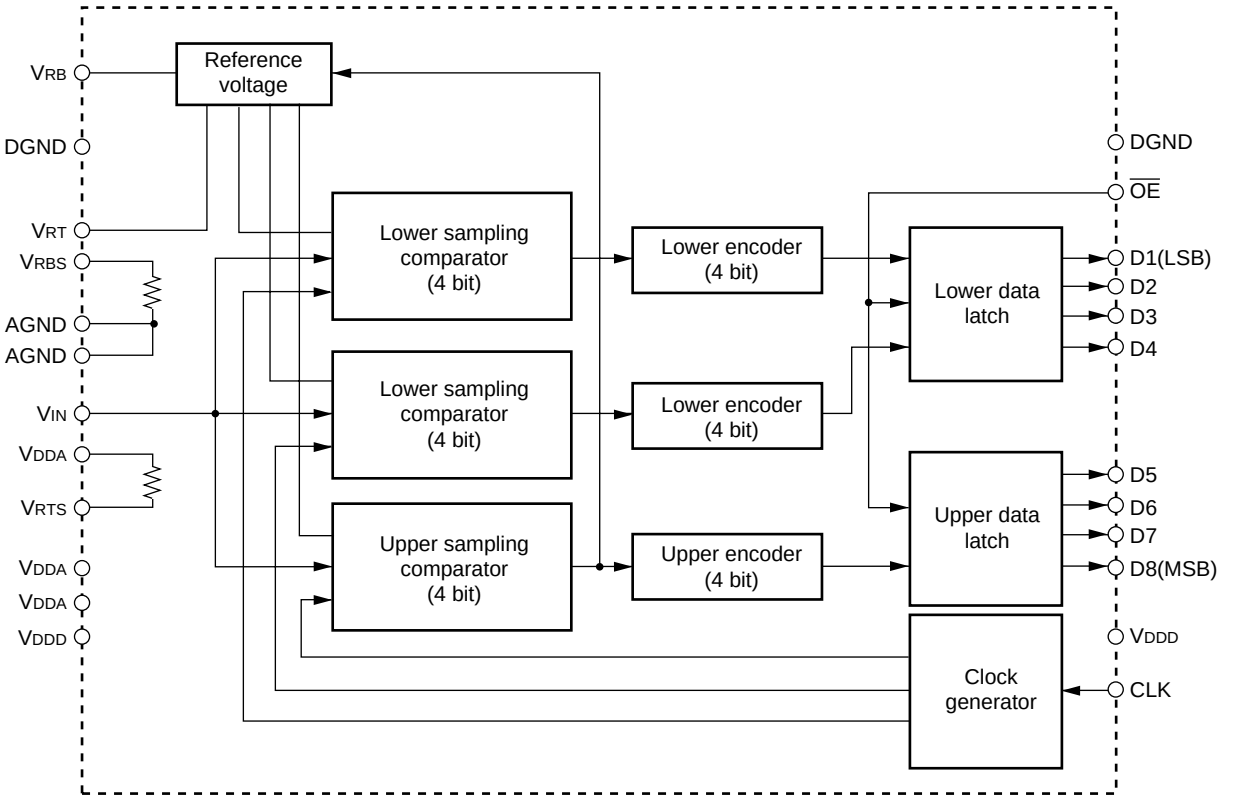


Fig. 6-6 CXD1175AM internal block diagram

2-3. Memory

HM530281RTT-20 (QX19, QX20, QX21) is a 2.5 Mbit field memory. The pin configuration of the IC is shown in Fig. 6-7 , terminal function in table 6-2 and internal block diagram in Fig. 6-8.

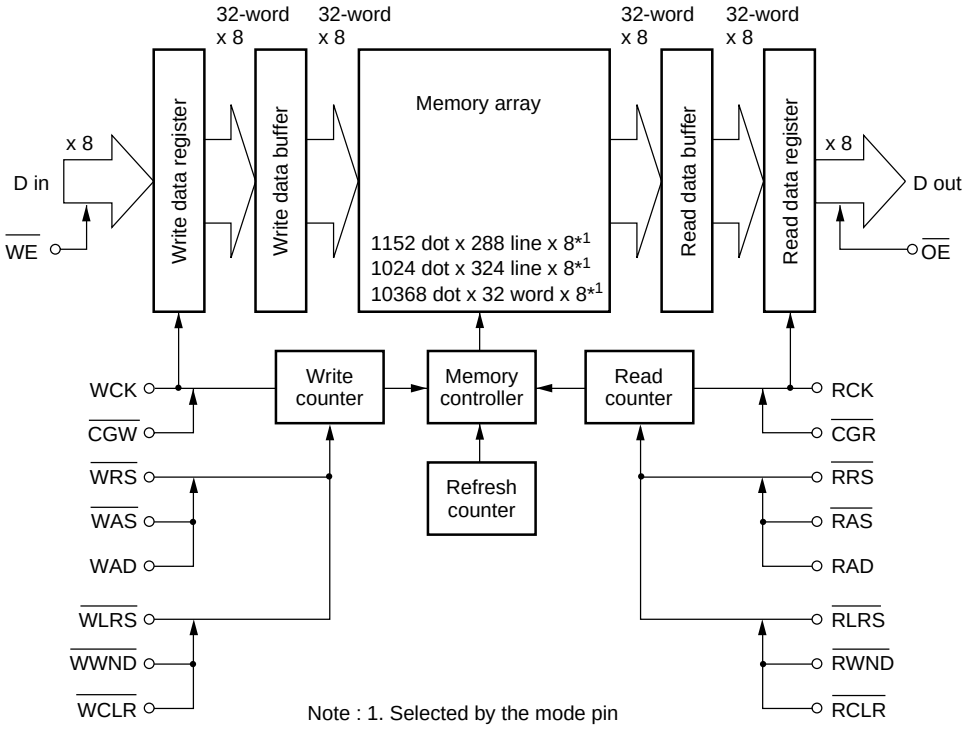


Fig. 6-8 HM530281RTT-20 internal block diagram

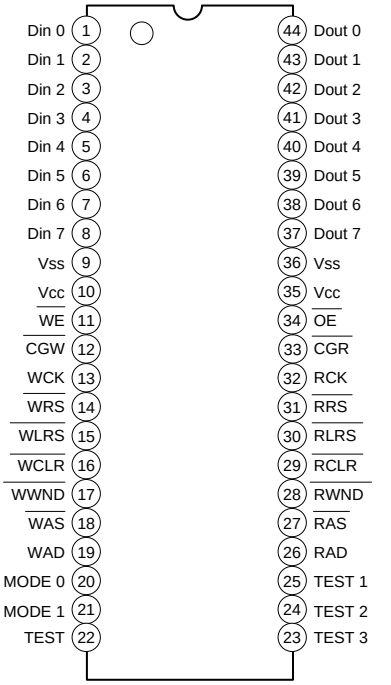


Fig. 6-7 HM530281RTT-20 pin function

Table 6-2 HM530281RTT-20 pin configuration

Pin No.	Name	Function	Pin No.	Name	Functions
1 - 8	D_{IN0-7}	Data input	22 - 25	TEST 0 - 3	Connect to GND.
9	V_{SS}	GND	26	RAD	Read address
10	V_{CC}	Power supply voltage	27	$\overline{RAS}$	Read address set
11	$\overline{WE}$	Write enable	28	$\overline{RWND}$	Read window mode
12	$\overline{CGW}$	Write clock gate	29	$\overline{RCLR}$	Read clear
13	$\overline{WCK}$	Write clock	30	$\overline{RLRS}$	Read line reset
14	$\overline{WRS}$	Write reset	31	$\overline{RRS}$	Read reset
15	$\overline{WLRS}$	Write line reset	32	RCK	Read clock
16	$\overline{WCLR}$	Write clear	33	$\overline{CGR}$	Read clock gate
17	$\overline{WWND}$	Write window mode	34	$\overline{OE}$	Output enable
18	$\overline{WAS}$	Write address set	35	V_{CC}	Power supply voltage
19	WAD	Write address	36	V_{SS}	GND
20 - 21	MODE 0 - 1	Mode selection input	37 - 44	D_{OUT0-7}	Data output

The IC has a screen applicable address mode which allows the access by specifying a horizontal and vertical addresses in addition to the one-dimension address mode which works as FIFO.

The control in each mode is determined by the condition of MODE 0 (pin 20) and MODE 1 (pin 21) when the power is turned on and the modes are set as shown in table 6-3.

Table 6-3

Mode 0	Mode 1	Address mode	Address configuration	Capacity
0	0	1 dimension	0 - 10367 block	331776 word
1	0	Screen application (1)	32 block (H) x 324 line (V)	1024 dot x 324 line
0	1	Screen application (2)	36 block (H) x 288 line (V)	1152 dot x 288 line

In the unit, the address 1 mode corresponding to screen is used. 1024 (H) x 324 (V) x 8 bits address corresponding to the screen are provided. The line hold reset which returns to the head of the current line and the line increment reset which goes forward to the head of the next line are provided other than the normal reset which jumps to the upper left address of the screen. (Refer to Fig. 6-9.)

These reset functions are controlled by the signal developed from pins 30 (RLRS), 31 (RRS) and 14 (WRS). Table 6-4 shows the relation of each reset terminal and reset function.

The write control to the memory is carried out by SYG (QX32) and the read control is by PLD (QX41). The write control signal timing is shown in Fig. 6-10 and the reset operation is carried out at the beginning of a field and the line increment reset is carried out at the beginning of every line. The read control is described in the next item “2-4. PLD Circuit”.

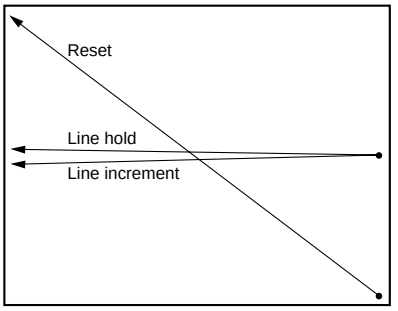


Fig. 6-9 HM530281RTT reset operation

Table 6-4 Each reset terminal and its operation

Level at RCK rising timing Mode 1		Operation mode	Functions
RRS	RLRS		
H	H	Normal mode	Increment syncronizing with RCK.
L	H	Reset	Reset to upper left of screen.
H	L	Line increment reset	Reset to head of next line.
L	L	Line hold reset	Reset to head of current line.

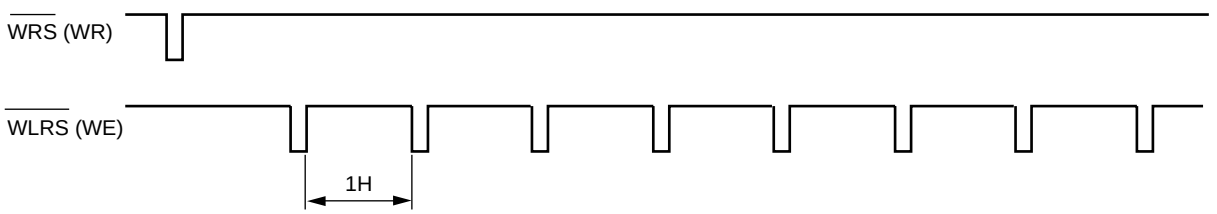


Fig. 6-10 Write control signal timing diagram

2-4. PLD Circuit

EPM7032LC44-10 is used for PLD (QX41). This PLD is based on CMOS EE-PROM and a device which can be written and erased electrically. The block diagram of the circuit written in the IC is shown in Fig. 6-11 and its pin configuration is shown in table 6-5. The IC is composed of the divider circuit, which operates PLL circuit (2), and memory control circuit.

In the divider circuit, the clock signal divided in four is output in the standard mode (including PAL/SECAM mode, pin 43 (MAG) develops high) and the clock signal divided in five is output in the enlargement mode (NTSC).

In PLL circuit (2), a clock signal dividing the clock signal generated in PLL circuit (1), in eight is input to the other end of an input terminal, so the clock signal with twice frequency is generated in the standard mode and the clock signal with 2.5 times frequency is generated in the enlargement mode.

In the memory control circuit, the memory read operation is controlled. The control method of the memory is shown in Fig. 6-12. The RR (read reset) signal for a field shown in the input signal section in Fig. 6-12 and the RE signal output once 1H are also input from SYG. (The RE signal stands for read enable signal originally, however, it is regarded as a HD signal for this unit.)

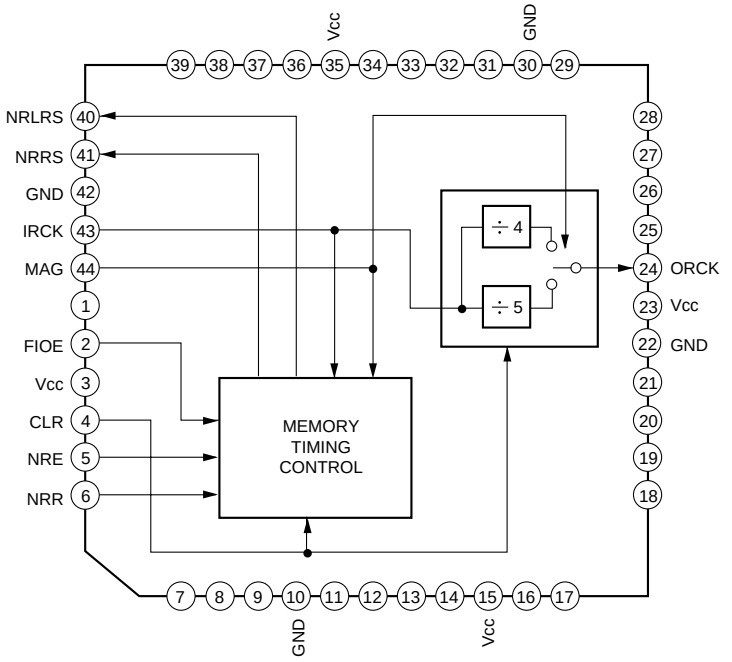


Fig. 6-11 EPM7032LC44-10 internal block diagram

These signals of clock signal for read (pin 43), enlargement control signal (pin 44) and field ID signal (pin 2) control the memory are shown in Fig. 6-12.

In the standard mode, after resetting the memory, the line increment reset and line hold operations are carried out alternately.

When the line hold operation is carried out, the same line is read twice repeatedly, so it is possible to convert the interlace signal into non-interlace signal. The line being read twice repeatedly is changed by ODD/EVEN of the field in order to correct the center of the interlace signal.

In the enlargement mode, after resetting the memory, the line hold operation once between the line increment operations and the line hold operation twice between the line increment operations are carried out alternately.

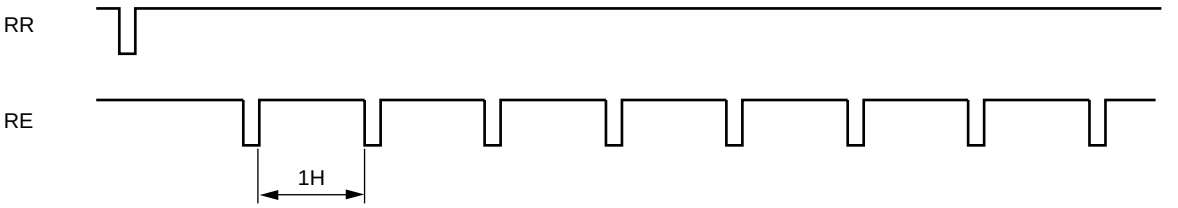
The operation is equivalent to convert one line into 2.5 lines, because the same line is read repeatedly twice and three times alternately. In this operation, twice conversion of the non-interlace signal conversion is included, so the picture is enlarged 1.25 times in the vertical direction. In this case, the operation pattern is also shifted by 1 line by the ODD/EVEN of a field to perform the center correction for the interlace signal. In this kind of conversion, shaggy lines may be conspicuous at a slanted portion because a line is simply enlarged repeatedly.

Pin 4 (CLR) controls all output terminals of the PLD to low. When a signal comes from a personal computer, this terminal is set to Hi to stop the PLD operation.

Table 6-5 EPM7032LC44-10 pin function

Pin No.	Name	Functions
2	FIOE	Field ODD/EVEN ID signal (ODD: Lo)
4	CLR	Output clear input terminal (All outputs become Lo when Hi.)
5	NRE	RE (Read Enable) signal input terminal
6	NRR	RR (Read Reset) signal input terminal
24	ORCK	Clock output terminal (PLL (2))
40	NRLRS	RLRS (Read Line Reset) signal output terminal
41	NRRS	RRS (Read Reset) signal output terminal
43	IRCK	Clock input terminal
44	MAG	Enlargement control signal output terminal

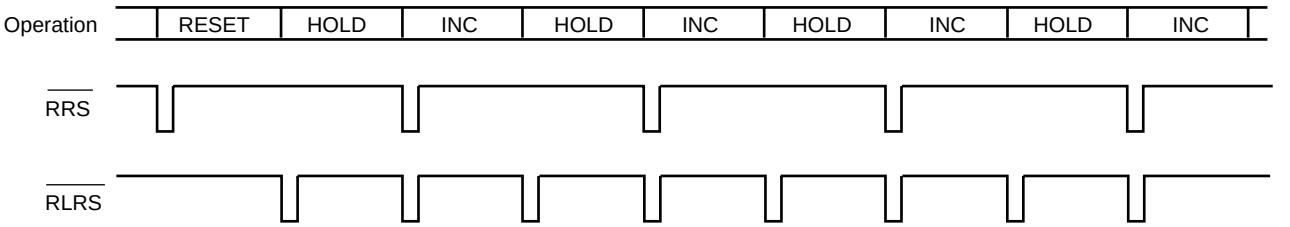
< Input signal >



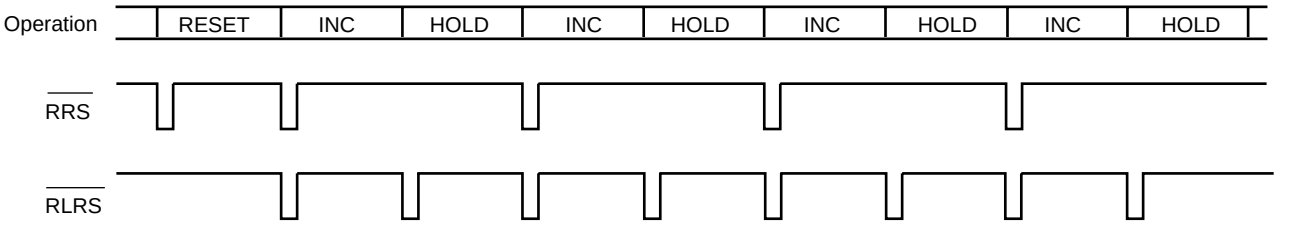
< Output signal >

NTSC (Standard) • PAL • SECAM (MAG=L)

FIOE=L (ODD FIELD)

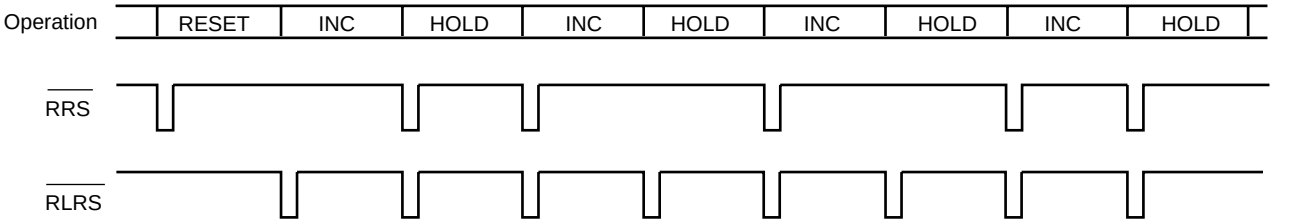


FIOE=H (EVEN FIELD)



NTSC (Enlargement) (MAG=H)

FIOE=L (ODD FIELD)



FIOE=L (EVEN FIELD)

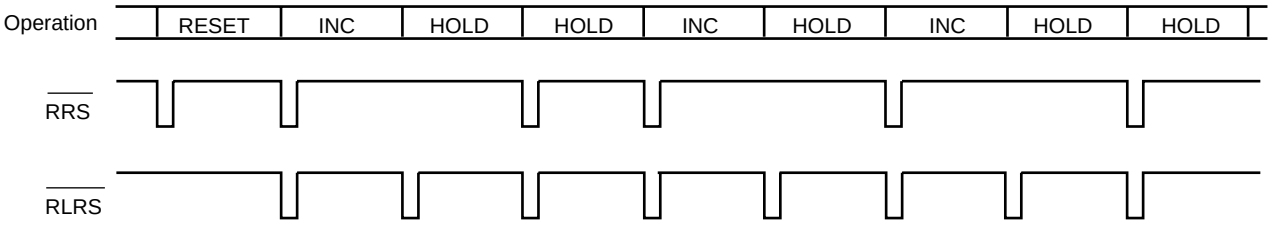


Fig. 6-12 Memory control signal timing diagram

2-5. D/A Converter

MB40958PF is a 8-bit/3ch bi-polar D/A converter which works at a conversion rate of 60 M sample/s. The pin configuration of the IC is shown in Fig. 6-13, the pin functions are in table 6-6 and its internal block diagram is in Fig. 6-14. The peripheral circuit of the D/A converter is shown in Fig. 6-15.

The reference voltage output terminal is connected to the reference voltage input terminal (pin 37) and supplied with 3V. Accordingly, the output signal amplitude is 2V varying from 3 to 5V. The RGB signals output from pins 46, 43 and 40 pass through two stages of emitter follower buffers and then output from the digital circuit.

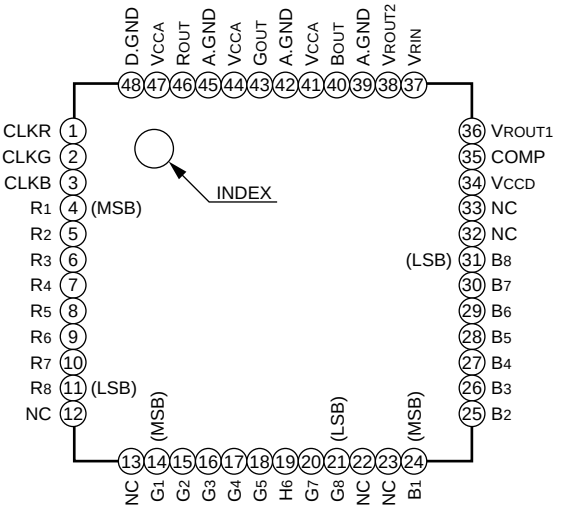


Fig. 6-13 Pin configuration of MB40958PF

Table 6-6 Pin function of MB40958PF

Pin No.	Name	I/O	Function
1	CLKR	I	R channel clock signal input terminal
2	CLKG	I	G channel clock signal input terminal
3	CLKB	I	B channel clock signal input terminal
4 ~ 11	R1 ~ R8	I	R channel data signal input terminal. (R1: MSB, R8: LSB)
14 ~ 21	G1 ~ G8	I	G channel data signal input terminal. (G1: MSB, G8: LSB)
24 ~ 31	B1 ~ B8	I	B channel data signal input terminal. (B1: MSB, B8: LSB)
34	V_{CCD}	-	Digital power supply terminal (+5V)
41, 44, 47	V_{CCA}	-	Analog power supply terminal (+5V)
48	D.GND	-	Digital ground terminal (0V)
39, 42, 45	A.GND	-	Analog ground terminal (0V)
37	V_{RIN}	I	Reference voltage input terminal for setting analog output dynamic range. When using the internal reference voltage, connect this terminal to pin 36 or 38. When using the external reference voltage, the voltage range should be within 2.65V ~ 4.3V and V_{CCA} - V_{RIN}= 0.7V ~ 2.2V.
36	V_{ROUT1}	O	Reference voltage output terminal 1 for resistance separation. Output voltage is set to 0.6 x V_{CCA}. When connecting to pin 37, 0.6 x V_{CCA} ~ V_{CCA} analog output voltage is obtained.
38	V_{ROUT2}	O	Reference voltage output terminal 2 for band gap reference. Output voltage is set to V_{CCA} - 2V. When connecting to pin 37, V_{CCA} - 2V ~ V_{CCA} analog output voltage is obtained.
35	COMP	-	Phase compensation capacitance terminal. A capacitor of 0.1µF or more shall be connected between A.GND.
46	R_{OUT}	O	R channel analog output terminal.
43	G_{OUT}	O	G channel analog output terminal.
40	B_{OUT}	O	B channel analog output terminal.
12, 13, 22, 23, 32, 33	N.C.	-	Nonconnected terminal.

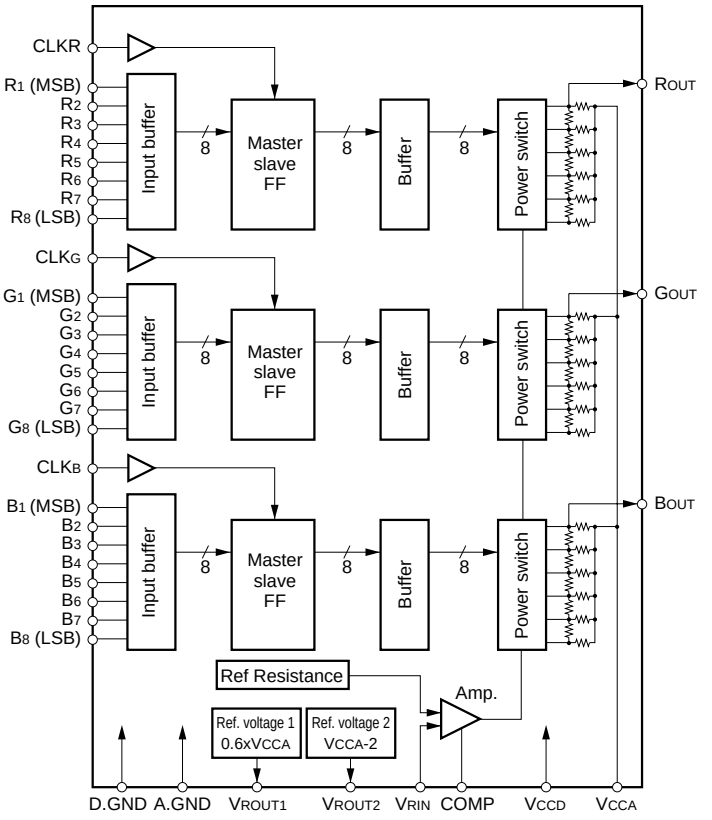


Fig. 6-14 MB40958PF internal block diagram

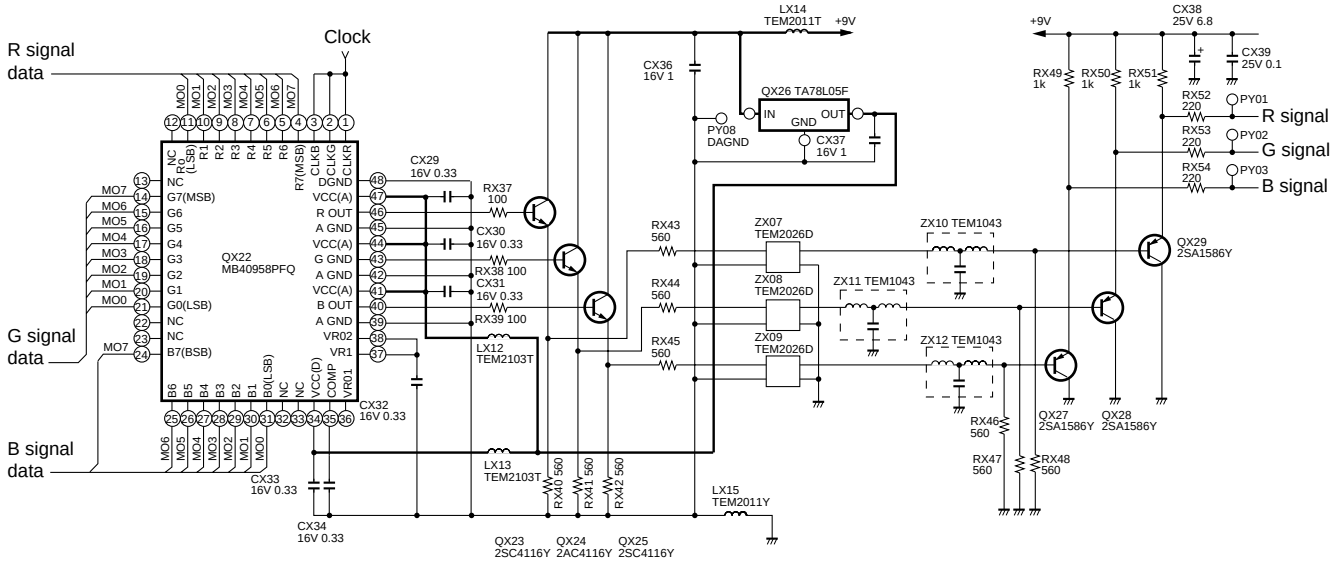


Fig. 6-15 D/A converter peripheral circuit

2-6. Memory Control and Sync Process IC

TC160G54AF1137 (usually called SYG, QX32) is an gate array which carries out the memory control and sync process. SYG is entirely composed of 4 sections as shown in Fig. 6-16; write timing generation section, read timing generation section, sync signal measurement section and serial bus interface section.

In the write timing generation circuit, the clock signal input to pin 149 is divided and HD signal for PLL (1) is generated at pin 128. In the PLL (1), the signal and HD signal sent from external circuit are compared and a clock signal synchronized with the input signal is generated. PLL (1) loop circuit is formed by returning the clock signal to the write timing circuit through pin 149 after divided in four. Also, in the write timing circuit, write control signal for a memory is generated.

In the read timing generation circuit, the memory read control signal and the reference timing signal for on-screen generation circuit and liquid crystal panel timing generation circuit are generated.

A clock signal used in the memory read timing control circuit operation can be used by switching the clock signal generated in the PLL circuit (1) (divided in four) and the clock signal generated in PLL circuit (2) with the serial bus setting.

When a signal is sent from a personal computer, the clock signal from PLL circuit (1) is used and when a NTSC/PAL signal is sent, the clock signal from PLL circuit (2) is used.

In the sync signal measurement section, a HD signal frequency input to pin 134 and line number for 1 field is measured. The measured data is read to the microcomputer through the serial bus and used for the personal computer signal automatic identification. For the measurement reference signal, 25.18 MHz clock signal is used.

In the serial bus interface section, the data transmission between the IC and the microcomputer is carried out. The serial bus format is of a three line bus type using R/W (pin 44), DATA (pin 43) and CLOCK (pin 42). For the serial bus format system, refer to item 12 in section 5.

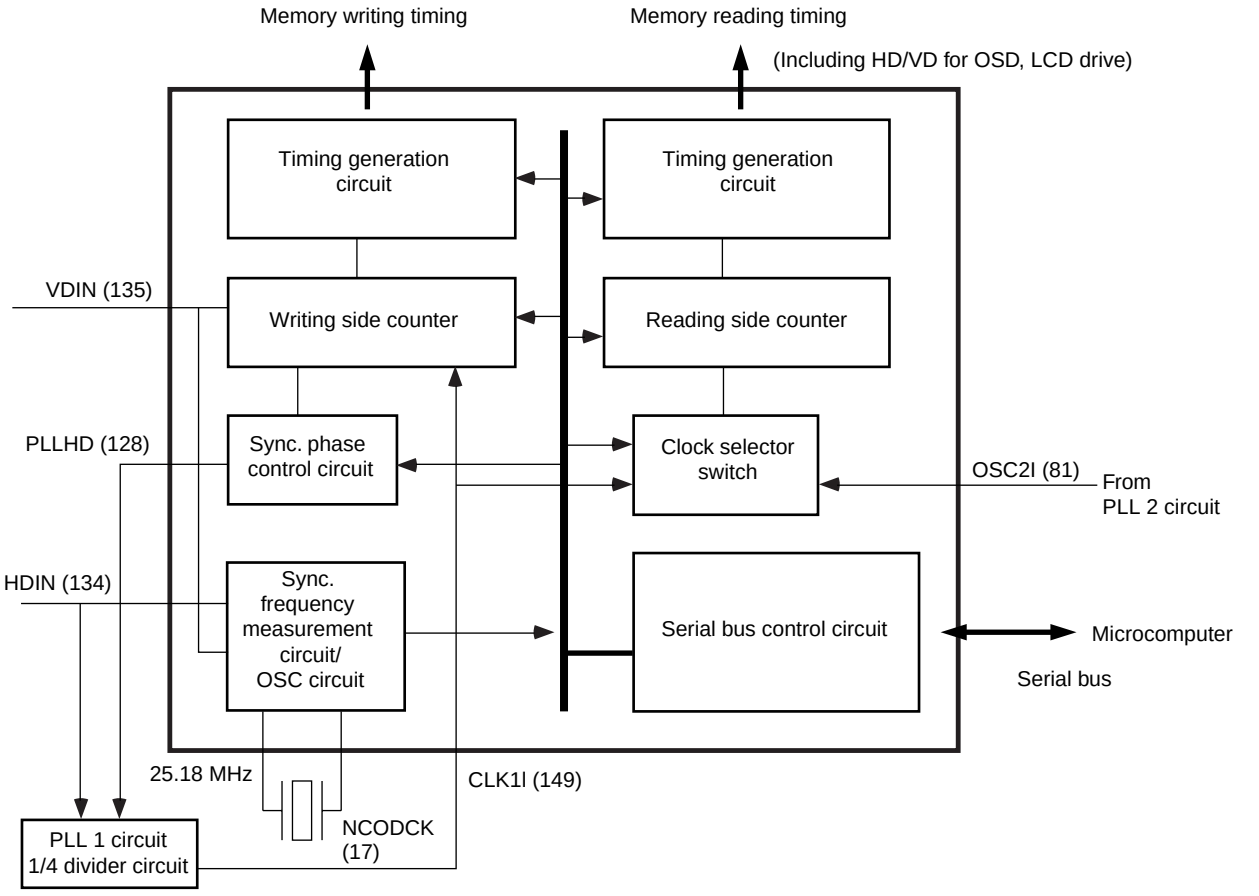


Fig. 6-16 TC160G54AF1137

2-7. PLL Circuit (1)

TLC2933IPW is used in the PLL circuit. The pin configuration is shown in Fig. 6-17, the terminal functions are in table 6-7 and the internal block diagram is shown in Fig. 6-18. The circuit diagram for the PLL circuit is shown in Fig. 6-19. The IC is composed of a VCO able to lock in 40 – to 100 MHz and PFD. In this unit, a perfect integration type loop filter is provided by combining the IC and an op. amplifier (Q701, M33087M).

The center frequency of VCO varies depending on the constant value of R708, and with 3.3 kW selected the lock enable frequency is approx. 40 – 85 MHz.

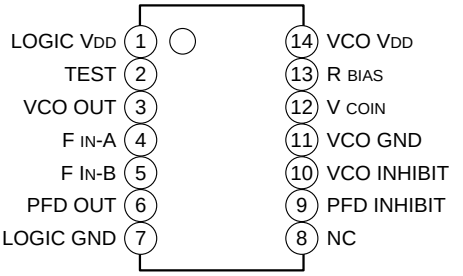


Fig. 6-17 Pin configuration of TLC2933IPW

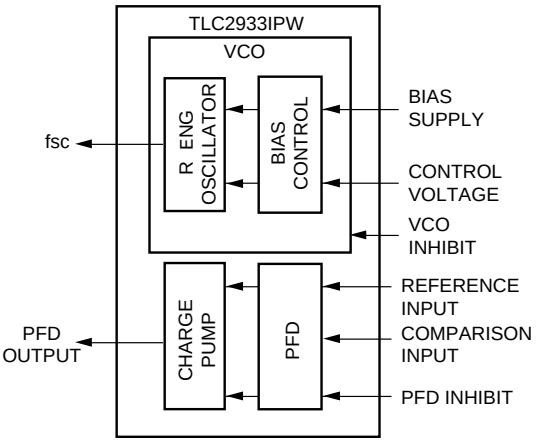


Fig. 6-18 TLC2933IPW internal block diagram

Table 6-7 TLC2933IPW pin function

Pin No.	Name	Function
1	LOGIC V_{DD}	Power supply voltage supply terminal for internal logic circuit (PFD section, I/O section). Desirable to be separated from power supply voltage supply terminal for VCO completely.
2	TEST	Used at test. Connect to GND at normal operation.
3	VCO OUT	VCO output terminal. Fixed to "L" level at inhibit.
4, 5	F_{IN} - A, F_{IN} - B	Input terminal for reference frequency input (f_{REF}-IN) and comp. signal dividing VCO output by external counter. Input f_{REF}-IN to F_{IN}-A terminal at rag-read filter use and comp. signal from external counter to F_{IN}-B.
6	PFD OUT	PFD output terminal. Fixed to high impedance at PFD ihibit.
7	LOGIC GND	GND terminal for internal logic circuit
8	N.C.	Internal not connected terminal.
9	PFD INHIBIT	PFD inhibit function control terminal.
10	VCO INHIBIT	VCO inhibit function control terminal.
11	VCO GND	VCO GND terminal
12	V_{CDIN}	VCO control voltage input terminal. Normally input VCO oscillation control voltage from LPF output formed at external circuit.
13	R_{BIAS}	VCO bias supply resistor connection terminal. Supply bias to operate VCO oscillation and insert a resistor between the terminal and VCO power supply line in order to set/adjust the oscillation frequency range.
14	VCO V_{DD}	VCO power supply voltage supply terminal. Desirable to be separated from power supply voltage supply terminal for internal logic.

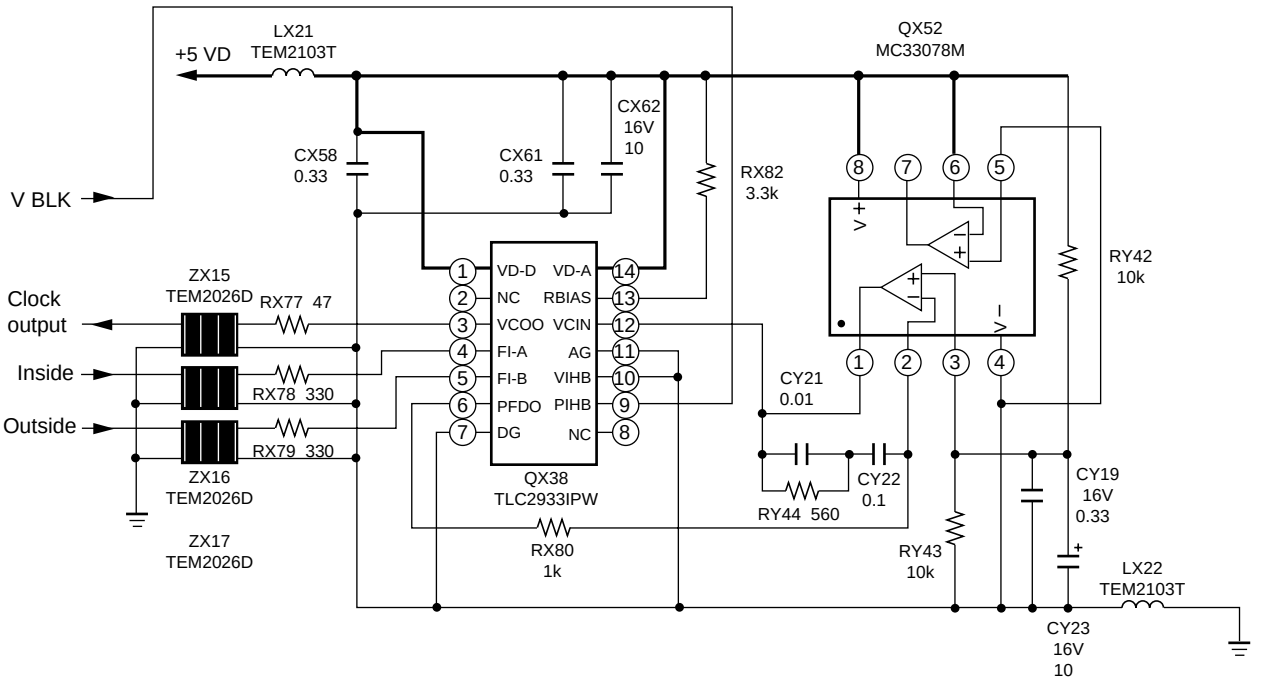


Fig. 6-19 PLL Circuit (1) circuit diagram

2-8. PLL Circuit (2)

TLC2932IPW (QX42) is used in the PLL circuit. The pin configuration is shown in Fig. 6-20, the terminal functions are in table 6-8 and the internal block diagram is shown in Fig. 6-21.

The circuit diagram of PLL circuit is shown in Fig. 6-23.

The IC is composed of a VCO able to oscillate in 20 – 60 MHz and PFD. In this unit, a rag-read type loop filter is provided by combining the IC and CRs. The center frequency of VCO varies depending on the constant value of RX88 and the lock enable frequency is approx. 23 – 40 MHz when the RX88 is 3.3 kW.

VHB (pin 10) and PIHB (pin 9) are the terminals to stop the VCO/PFD operation. To display signal sent from the personal computer, the IC operation is stopped by making these terminals Hi.

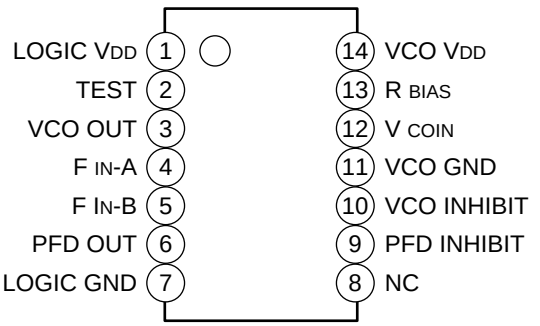


Fig. 6-20 Pin configuration of TLC2932IPW

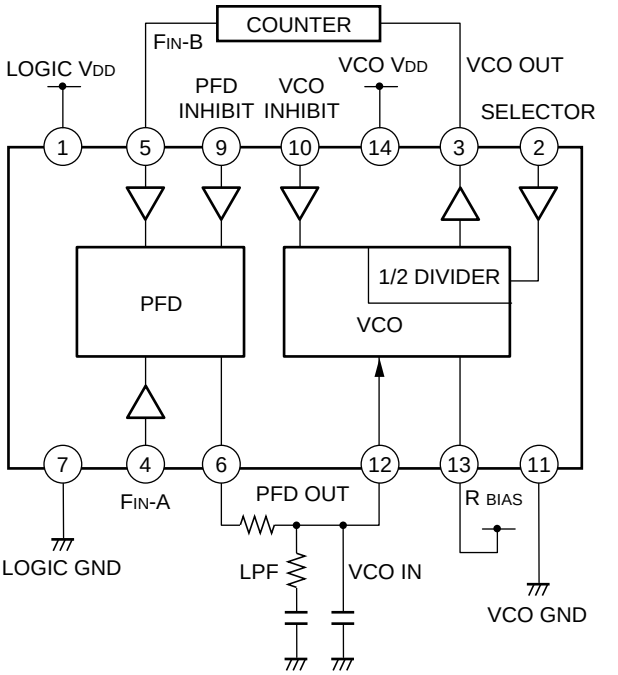


Fig. 6-21 TLC2932IPW internal block diagram

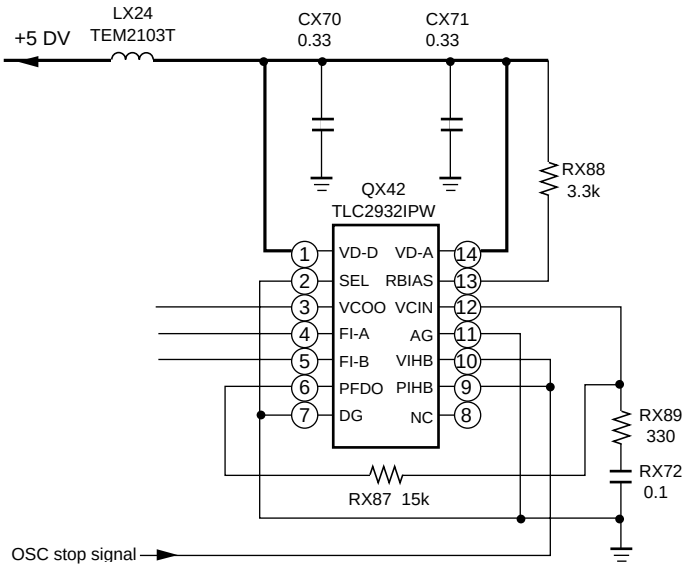


Fig. 6-22 PLL Circuit (2) circuit diagram

Table 6-8 TLC2932IPW pin function

Pin No.	Name	Function
1	LOGIC V_{DD}	Source voltage supply terminal for internal logic circuit. It is desirable that it is completely separated from the source voltage supply terminal of VCO.
2	SELECT	Output frequency 1/2 divider select terminal for VCO. VCO's output frequency can be divided into two to output by controlling this terminal with external logic.
3	VCO OUT	VCO output terminal. At inhibit, it becomes "L".
4, 5	F_{IN}-A, F_{IN}-B	Two input terminals for a detection of edge difference between the reference frequency (f_{REF} -IN) and frequency from the external counter. Normally, f_{REF}-IN is input at F_{IN}-A terminal, and the frequency from the external counter that is divided/multiplied is input at F_{IN}-B terminal.
6	PFD OUT	PFD output terminal. It can be fixed at high impedance.
7	LOGIC GND	GND terminal for internal logic circuit.
8	N.C.	Internal unconnected terminal.
9	PFD INHIBIT	PFD inhibit function control terminal.
10	VCO INHIBIT	VCO inhibit function control terminal.
11	VCO GND	VCO GND terminal.
12	V_{COIN}	VCO control voltage input terminal. In PLL, VCO generation control voltage is normally input from external LPF.
13	R_{BIAS}	Bias resistor connection terminal for VCO oscillation frequency setting. Bias resistor is connected in between power line and this terminal for setting/adjusting oscillation frequency and for a supply of bias for oscillation operation at internal VCO.
14	VCO V_{DD}	Source voltage supply terminal for VCO. It is desirable that this terminal be completely separated from the source voltage terminal for internal logic.

2-9. Liquid Crystal Panel Timing Generation Circuit

CXD2442Q (QX45) is a timing generation IC for the liquid crystal panel LCX016AL. The pin configuration of the IC is shown in Fig. 6-23, the terminal functions are in table 6-9, and the internal block diagram is shown in Fig. 6-24.

This IC generates all the timing necessary for the liquid crystal panel. The IC operation is controlled by the serial bus and the IC controls the up/down/left/right inversion and signal mode setting. The example of the timing signal generated in the IC is shown in Figs 6-25 and 6-26.

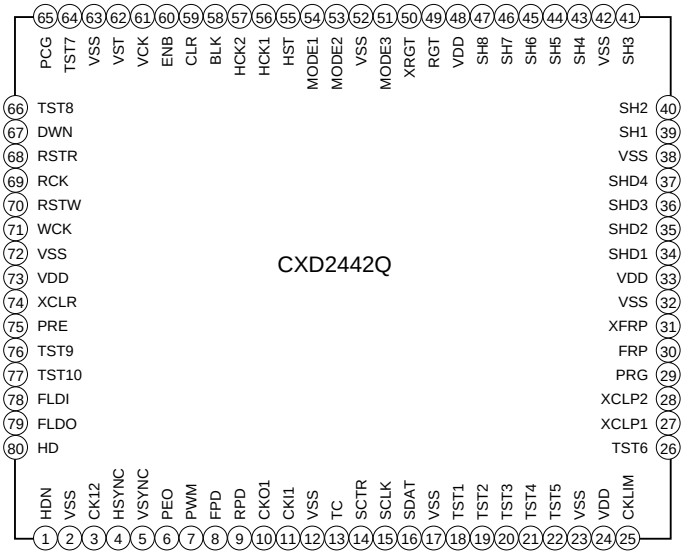


Fig. 6-23 Pin configuration of CXD2442Q

Table 6-9 CXD2442Q pin function

Pin No.	Name	I/O	Functions
1	HDN	O	Pulse output for phase comapration
2	V_{SS}	-	GND
3	CK12	I	Colck input terminal (VGA)
4	HSYNC	I	Horizontal sync signal input terminal
5	VSYNC	I	Vertical sync signal input terminal
6	PEO	I/O	Integrator output terminal for loop filter (AV)
7	PWM	I	Integrator input terminal for loop filter (AV)
8	FPD	O	Phase comparator output terminal (AV)
9	RPD	O	Phase comparator input terminal (AV)
10	CKO1	I/O	Oscillation cell output terminal (AV)
11	CKI1	I	Oscillation cell input terminal (AV)
12	V_{SS}	-	GND
13	TC	I/O	FPD output pulse width adjustment terminal
14	SCTR	I	Chip select input terminal (Serial transmission section)
15	SCLK	I	Serial clock input terminal (Serial transmission section)
16	SDAT	I	Serial data input terminal (Serial transmission section)
17	V_{SS}	-	GND
18	TST1	-	Test terminal (Open when used)
19	TST2	-	Test terminal (Open when used)
20	TST3	-	Test terminal (Open when used)

Pin No.	Name	I/O	Functions
21	TST4	-	Test terminal (Open when used.)
22	TST5	-	Test terminal (Connect to GND.)
23	V_{SS}	-	GND
24	VDD	-	Power supply
25	CKLIM	I	CKI1 input limit input terminal (H: CKI1 input possible, L: impossible)
26	TST6	-	Test terminal (Open when used.)
27	XCLP1	O	Pulse 1 output for pedestal clamp (Negative polarity)
28	XCLP2	O	Pulse 2 output for pedestal clamp (Negative polarity)
29	PRG	O	Pulse output for pre-charge signal
30	FRP	O	Alternative current drive inversion timing output (Inverted polarity to XFRP)
31	XFRP	-	Alternative current drive inversion timing output (Inverted polarity to FRP)
32	V_{SS}	-	GND
33	V_{DD}	-	Power supply
34	SHD1	O	Sample and hold pulse 1 output (For driver, positive polarity)
35	SHD2	O	Sample and hold pulse 2 output (For driver, positive polarity)
36	SHD3	O	Sample and hold pulse 3 output (For driver, positive polarity)
37	SHD4	O	Sample and hold pulse 4 output (For driver, positive polarity)
38	V_{SS}	-	GND
39	SH1	O	Sample and hold pulse 1 output (For high withstanding voltage SH, positive polarity)
40	SH2	O	Sample and hold pulse 2 output (For high withstanding voltage SH, positive polarity)
41	SH3	O	Sample and hold pulse 3 output (For high withstanding voltage SH, positive polarity)
42	V_{SS}	-	GND
43	SH4	O	Sample and hold pulse 4 output (For high withstanding voltage SH, positive polarity)
44	SH5	O	Sample and hold pulse 5 output (For high withstanding voltage SH, positive polarity)
45	SH6	O	Sample and hold pulse 6 output (For high withstanding voltage SH, positive polarity)
46	SH7	O	Sample and hold pulse 7 output (For high withstanding voltage SH, positive polarity)
47	SH8	O	Sample and hold pulse 8 output (For high withstanding voltage SH, positive polarity)
48	V_{DD}	-	Power supply
49	RGT	O	Left and Right inversion identification signal output (H: Normal, L: Reverse)
50	XRGT	O	Left and Right inversion identification signal output (H: Reverse, L: Normal)
51	MODE3	O	MODE switch terminal 3 output
52	V_{SS}	-	GND
53	MODE2	O	MODE switch terminal 2 output
54	MODE1	O	MODE switch terminal 1 output
55	HST	O	H start pulse output
56	HCK1	O	H clock 1 pulse output
57	HCK2	O	H clock 2 pulse output
58	BLK	O	BLK pulse output (Positive polarity)
59	CLR	O	CLR pulse output (Positive polarity)
60	ENB	O	ENB pulse output (Negative polarity)

Pin No.	Name	I/O	Functions
61	VCK	O	V clock pulse output
62	VST	O	V start pulse output
63	V_{SS}	-	GND
64	TST7	-	Test terminal (Open when used.)
65	PCG	O	PCG pulse ouptput (Positive polarity)
66	TST8	-	Test terminal (Open when used.)
67	DWN	O	Up and down inversion identification signal output (H: down, L: up)
68	RSTR	O	Reset read output (For high speed line buffer, Negative polarity)
69	RCK	O	Read clock output (For high speed line buffer)
70	RSTW	O	Reset write output (For high speed line buffer, Negative polarity)
71	WCK	O	Write clock output (High speed line buffer)
72	V_{SS}	-	GND
73	V_{DD}	-	Power supply
74	XCLR	I	System clear terminal (L: all clear)
75	PRE	I	Preset terminal (L: Preset to Macintosh 17 mode)
76	TST9	-	Test terminal (Open when used.)
77	TST10	-	Test terminal (Open when used.)
78	FLDI	I	Field identification signal input
79	FLDO	O	Field identification signal output
80	HD	O	HD pulse output (Positive polarity)

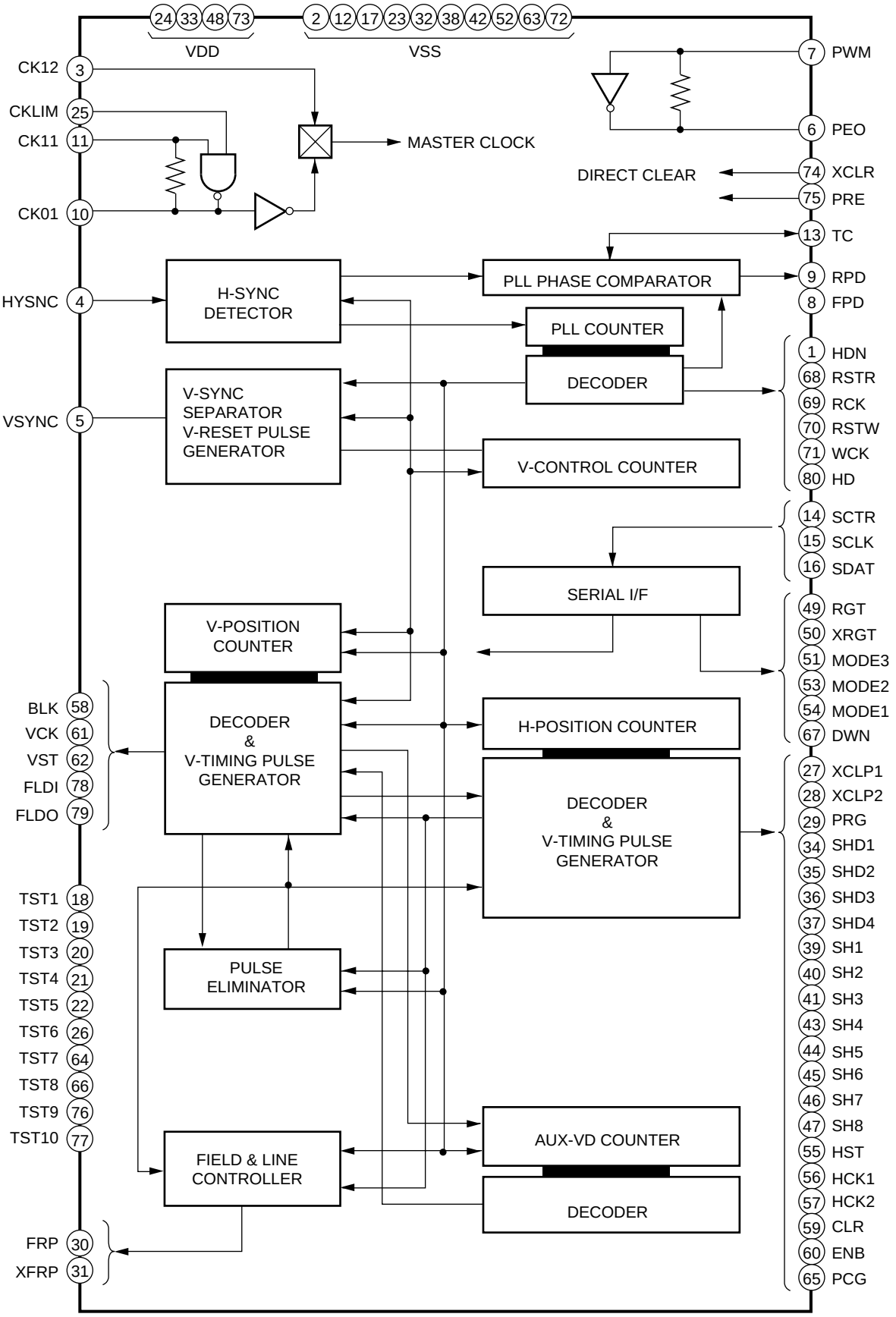
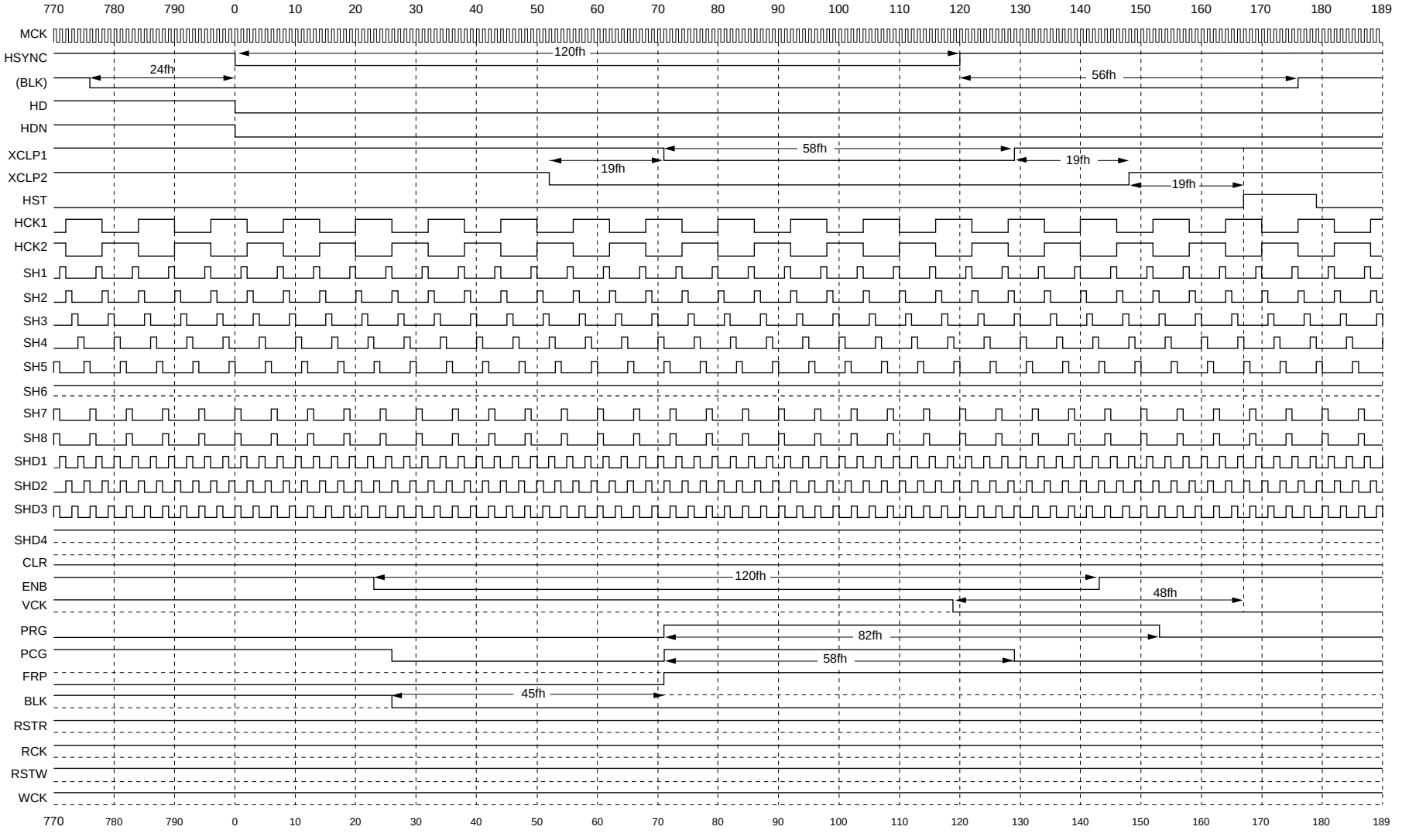


Fig. 6-24 CXD2442Q internal block diagram

LCX016 SVGA 800x600

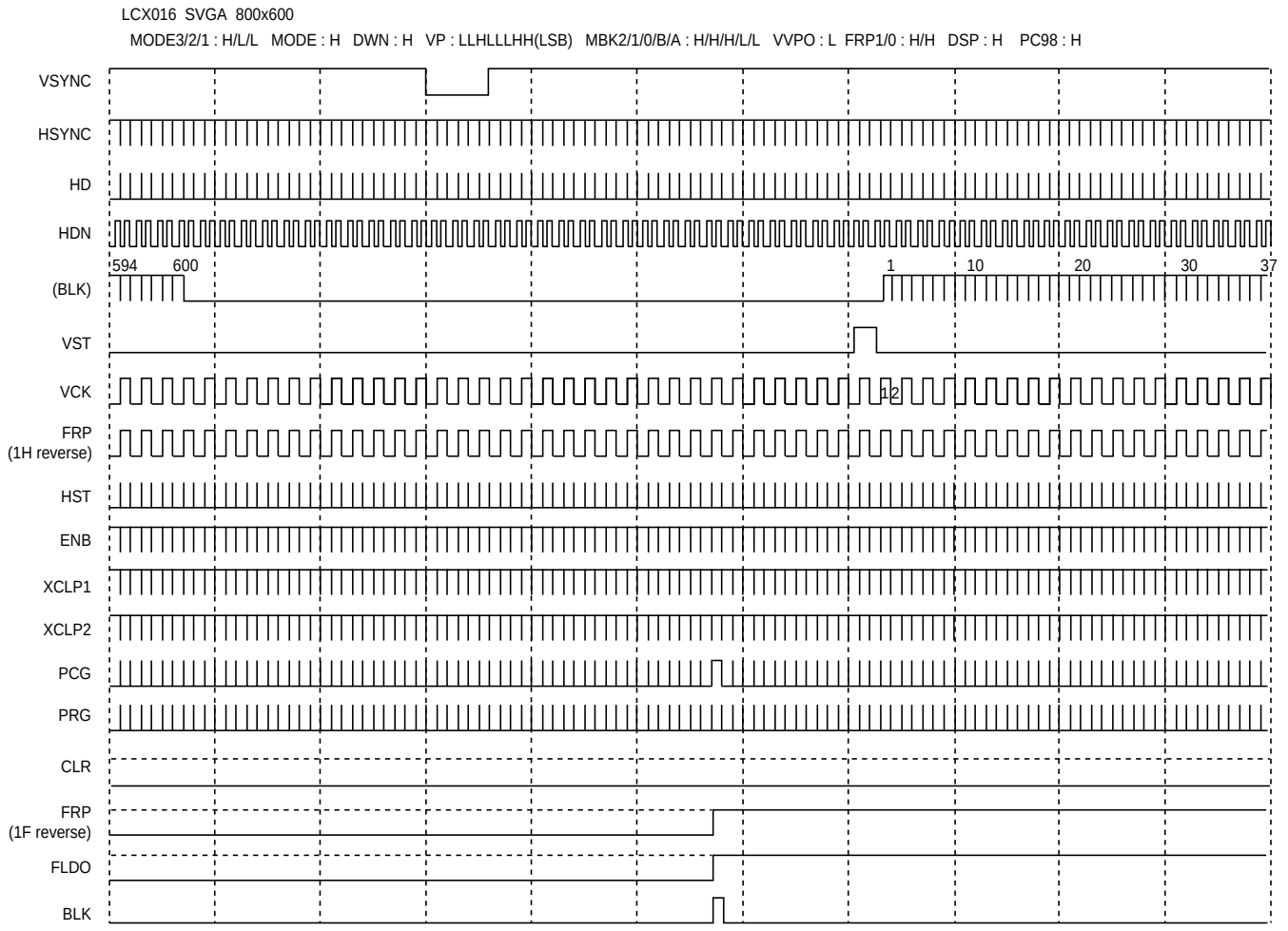
RGT : H PLLP : LHHHHHLLHLH(LSB) HP : HHHLHLLL(LSB) HDNP : LLLLL(LSB) SHP : LLLLLLL(LSB) HCKP : LLLL(LSB) Loop Counter : 999fh

HSTP : LH(LSB) CLPP : LL(LSB) SHD2/1/0 : L/H/H SH2/1/0 : H/L/H HPOL : L CK : L HR : H HST : H HST : H PCG : H MCK f : 48.00MHz(20.83ns)



Note : RGT : HCK1 and 2 are inverted at L. Pulse SH1, 2 and 3 are replaced to SH4, 5 and 6. SH1 is replaced with SHD3.
Upper third line (BLK) of the timing chart is not an actual pulse output from the terminal.
The pulse is drawn as temporary pulse to create the chart.

Fig. 6-25 Example of timing signal (1)



Note : DWN : VST is inverted at L. Upper fifth line (BLK) of the timing chart is not an actual pulse output from the terminal.
The pulse is drawn as temporary pulse to create the chart.
FRP/FCDO polarity for 1H and 1V frequency is not specified.

Fig. 6-26 Example of timing signal (2)

2-10. On-screen Character Generation Circuit

µPD6453GT (QX43) is an IC for the on-screen character generation function. The pin configuration of the IC is shown in Fig. 6-27, the terminal functions are in table 6-10 and the internal block diagram is in Fig. 6-28. The RGB signals for on-screen character display output from pins 12, 13 and 14 and the on-screen switching signal output from pin 15 are developed from the digital circuit and superimposed as a video signal in the RGB process circuit.

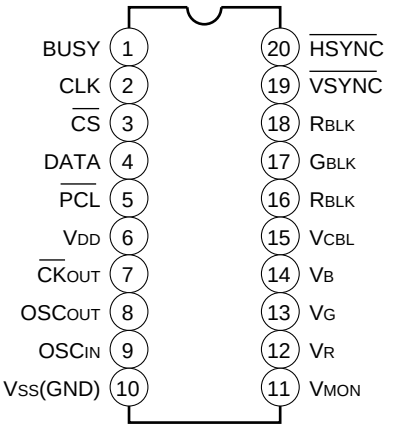


Fig. 6-27 Pin configuration of µPD6453GT

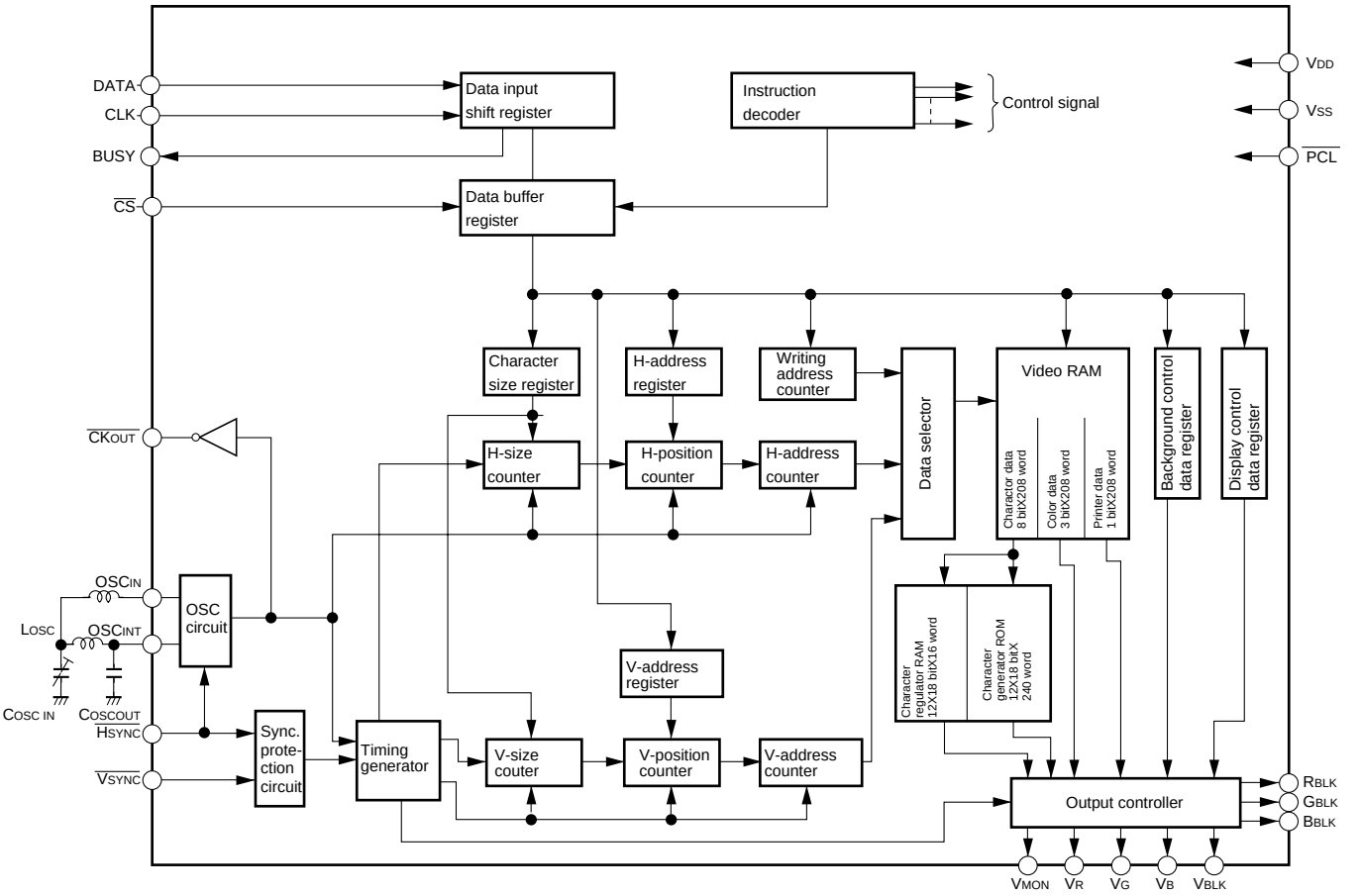


Fig. 6-28 µPD6453GT internal block diagram

Table 6-10 µPD6453GT pin function

Pin No.	Name	Terminal Name	Function
6	V_{DD}	Power supply terminal	Power supply (5V) terminal
10	V_{SS}	GND	Connect to system GND.
5	$\overline{PCL}$	Power on clear terminal	Clear terminal at power on. Set to L to H when power is turned on. VRAM lump-release start-up and test mode release operations are carried out.
4	DATA	Serial data input terminal	Control data input terminal
2	CLK	Clock input terminal	Clock input terminal for data read. Data which is added to DATA terminal at clock rising period is read.
3	CS	Chip select terminal	Serial transmission is acceptable by developing theis terminal from Hi to Low.
1	BUSY	BUSY signal output terminal	Serial data input possible/impossible detection terminal
8, 9	OSC_{IN} OSC_{OUT}	LC oscillation I/O terminal	I/O terminal for dot clock signal generation oscillator
7	$\overline{CK}_{OUT}$	Clock out terminal	Inverted output for OSC_{OUT}
20	$\overline{Hsync}$	Horizontal sync signal input terminal	Dot clock signal oscillator oscillates at signal rising period and sync Hi level.
19	$\overline{Vsync}$	Vertical sync signal input terminal	Input sync negative.
12, 13, 14	V_R V_G V_B	Character signal output terminal	Character signal output terminal corresponding to RGB signals. Signal output: Positive
15	V_{CBL}	Composite blanking output terminal	Blanking signal output terminal to cut video signals. 3 output composite signal for color corresponding blanking signal.
16, 17, 18	R_{BLK} G_{BLK} B_{BLK}	Character signal corresponding blanking output terminal	Blanking signal output terminal to cut video signals. RBLK, GBLK and BBLK are corresponding to the character signal outputs VR, VG and VB. Signal output: Positive
11	V_{MON} (MP)	Character signal monitor output terminal (mask pulse output terminal)	Output positive signal of the composite signals of VR, VG, VB. (Signal maks pulse is output as positive signal when selecting the mask pulse function in mask code option.

SECTION VII
VIDEO SIGNAL PROCESS CIRCUIT

1. OUTLINE

1-1. Circuit Configuration

The video signal process circuit consists of a video signal demodulation (NTSC, PAL, SECAM), RGB signal (VGA, SVGA) amplification and audio signal amplification circuits. Fig. 7-1 shows the block diagram.

1-2. Video Signal Demodulation Block

The video signal demodulation block demodulates the composite video signal and YC signal into the RGB signals.

The composite video signal is separated into a luminance signal (Y) and a color signal (C) in passing through a digital comb filter.

The YC signals selected by the input SW IC are processed in the Video/Color process IC and color difference signal delay circuits, and a Y color difference signal is created. At the same time the Y signal is corrected in its picture sharpness by the sharpness correction circuit and then fed to the RGB demodulation IC. The RGB demodulation IC develops R, G, and B signals.

1-3. RGB Signal Amplification Circuit Block

The RGB input signals are gain-adjusted in passing through the RGB process IC after the signals are switched to the RGB demodulated video signal, and then the RGB input signals are fed to the drive circuit provided in a later stage through the switching circuits.

The sync signal is corresponding to HD, VD, composite sync (CS) and SYNC ON G signals. The sync signal entered is separated into a HD and VD and waveform-shaped in the sync separation IC.

1-4. Audio Signal Amplification Block

Audio signal inputs are corresponding to L and R stereo inputs on the video and RGB inputs. The signals are output to the audio signal output terminals through the input SW IC. At the same time, the L and R signals are mixed, level adjusted in the volume control IC, and amplified by the audio output IC to a sufficient level to drive the speaker.

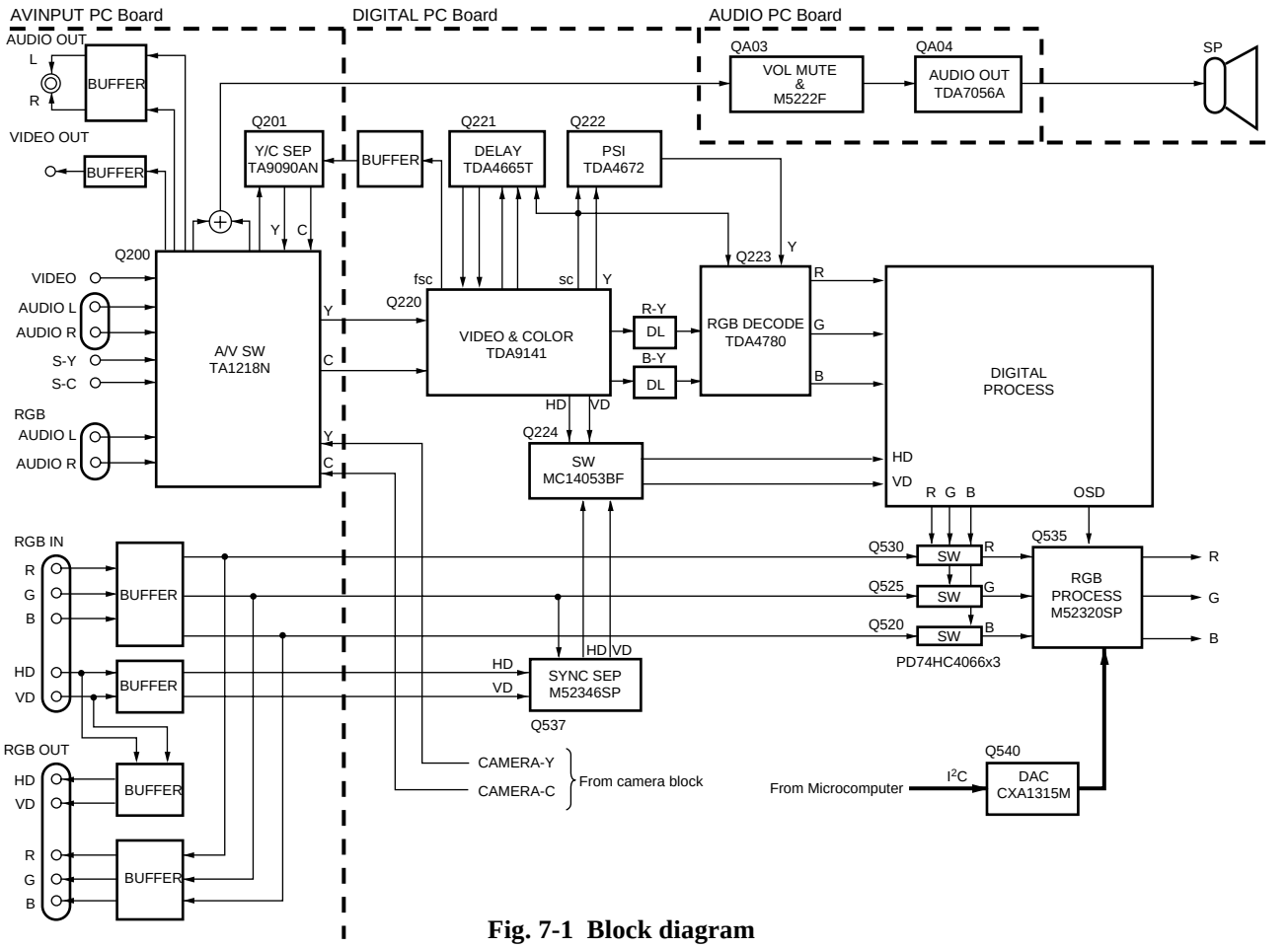


Fig. 7-1 Block diagram

2. INPUT/OUTPUT SIGNAL SWITCH CIRCUIT

The I/O signal switch circuit selects signals (video and audio) entered and feeds them to later stages and each output terminal. Fig. 7-2 shows the switching section of the audio/video signal switch circuit.

2-1. Audio/Video Signal Switch Circuit

The signal switching for the audio/video signal entered is carried out by Q200 SW IC (TA1218N). Each I/O signal is connected to Q200 as shown in Fig. 7-2. Each I/O control is entirely carried out through I^2C bus.

2-2. Input Signals

2-2-1. Composite Video Signal

The composite video signal is input to pin 10. When the composite video signal is selected, the composite video signal is output from pin 42 and supplied to Y/C separation circuit. The signal processed by Y/C separation circuit is input to pins 30 and 32 again, finally re-selected, and then output from pins 34 and 36.

2-2-2. S (Y/C) Signals

The Y/C signals input from S terminal are input to pins 12 and 14 respectively.

2-2-3. Camera Signal

The video signal sent from the camera section is supplied as Y/C signal and input to pins 16 and 18.

The video signal finally selected is output from pins 34 (C) and 36 (Y) respectively and supplied to the signal processing section in the later stage. At the same time, the same video signal as the finally selected video signal is output from pin 42 as a composite video signal. And then, the signal is output from the video output terminal through a buffer.

2-2-4. Audio Signal

The audio signal contains two kinds of input signals, video signal system and RGB signals. Each signal is corresponding to L and R stereo input signal system.

The audio signal for video signal is selected simultaneously when the composite video signal, S (Y/C) signal and camera signal are selected.

The audio signal for RGB signal system is selected when RGB signals are selected. The audio signals output from speakers after amplified through the amplifier section in the later stage are output from pins 35 (Rout 1) and 37 (Lout 1).

On the other hand, the audio signals output from the audio output terminals are output from pins 2 (Rout 2) and 1 (Lout 2). The signal selection method is the same as the audio signals fed to the speakers. The internal block diagram of Q200 SW IC (TA1218N) is shown in Fig. 7-2.

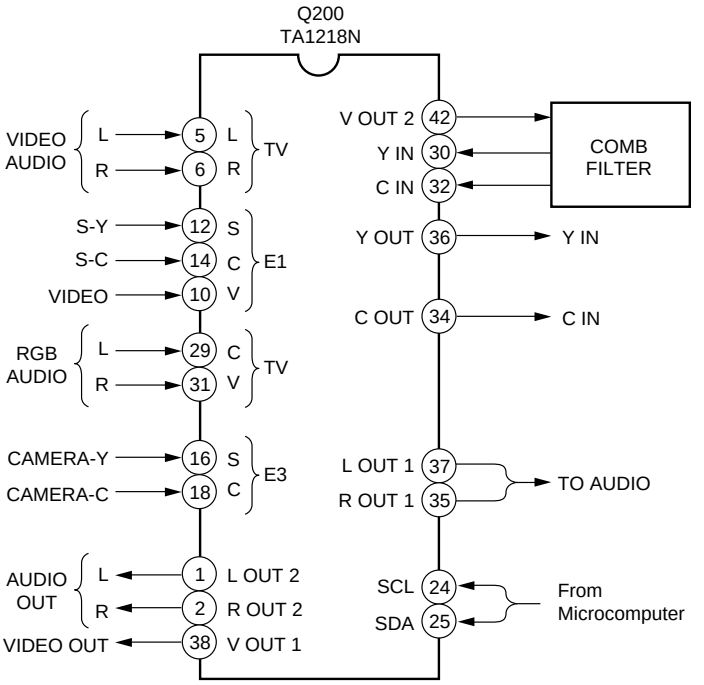


Fig. 7-2 Audio/video signal switch section

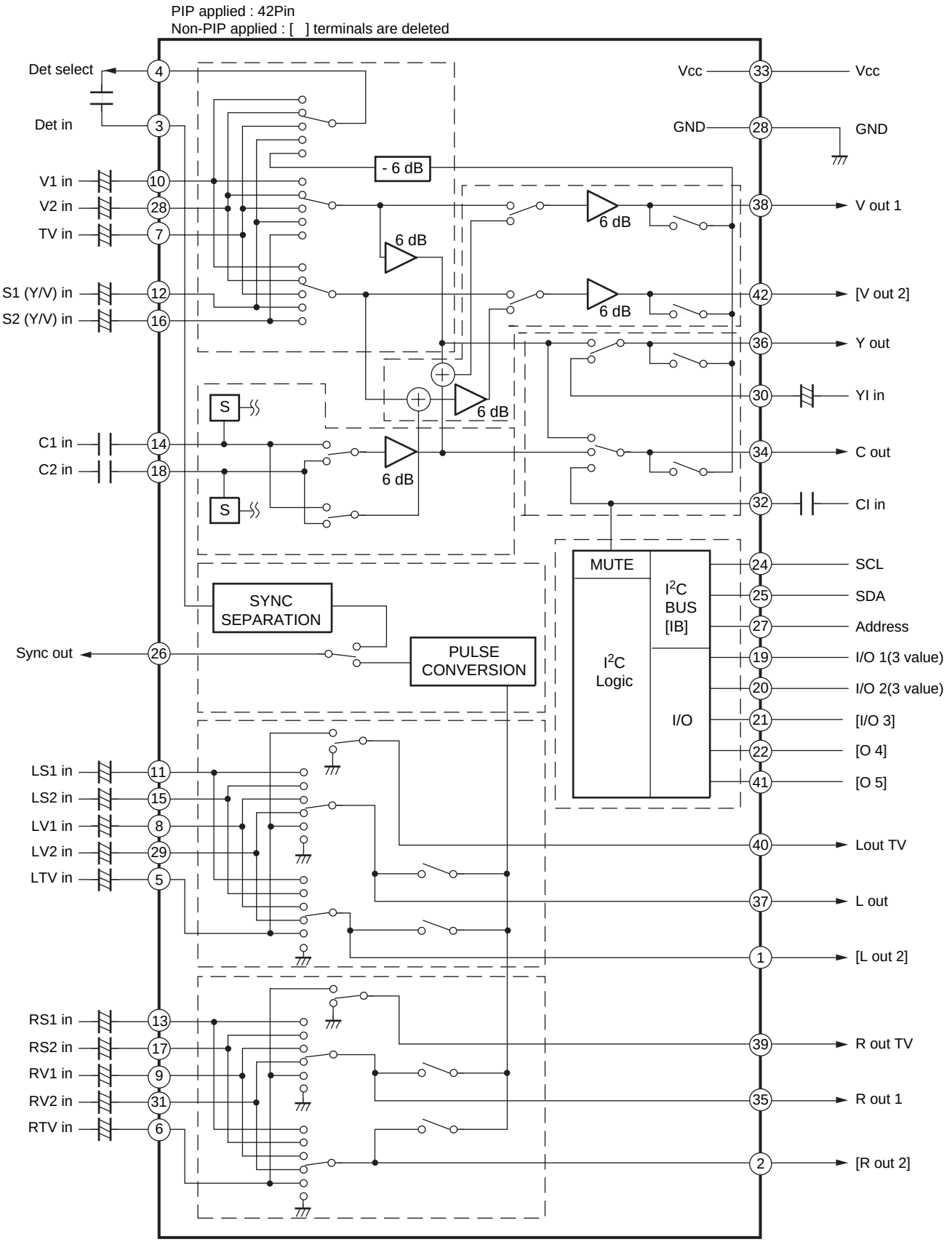


Fig. 7-3 Internal block diagram of TA1218N

3. VIDEO DEMODULATION BLOCK

3-1. YC Separation Circuit

This circuit separates Y and C signals from a composite video signal. Fig. 7-4 shows the pin configuration of TC9090AN and Fig. 7-5 shows the block diagram.

The composite video signal enters pin 3. A fsc (3.58/4.43MHz) output from the video/color IC enters pin 19 and is converted into a 4fsc of the drive clock frequency inside the IC. The composite video signal entered is processed at a rate of the clock frequency of the IC and output as Y and C signal.

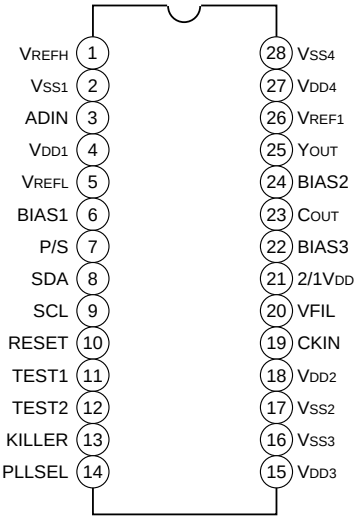


Fig. 7-4 Pin configuration of TC9090AN

Table 7-1 Terminal function of TC9090AN

Pin No.	Name	Function
1	V_{REFL}	ADC bias
2	V_{SS1}	ADC GND
3	ADIN	Video input
4	V_{DD1}	ADC V_{DD}
5	V_{REFH}	ADC bias
6	BIAS1	ADC bias
7	P/S	Selection function control
8	SCL	I^2C bus clock input
9	SDA	I^2C bus data input, check output
10	RESET	I^2C bus reset
11	TEST1	Test terminal
12	TEST2	Test terminal
13	KILLER	Clock killer switch
14	PLLSEL	Selection input clock
15	V_{DD3}	Digital V_{DD}
16	V_{SS3}	Analog GND
17	V_{SS2}	PLL GND
18	V_{DD2}	PLL V_{DD}
19	CKIN	Clock input
20	VFIL	VCO filter
21	2/1 V_{DD}	Line memory bias
22	BIAS3	DAC bias
23	C_{OUT}	C output
24	BIAS2	DAC bias
25	Y_{OUT}	Y output
26	V_{REF1}	DAC bias
27	V_{DD4}	DAC V_{DD}
28	V_{SS4}	DAC GND

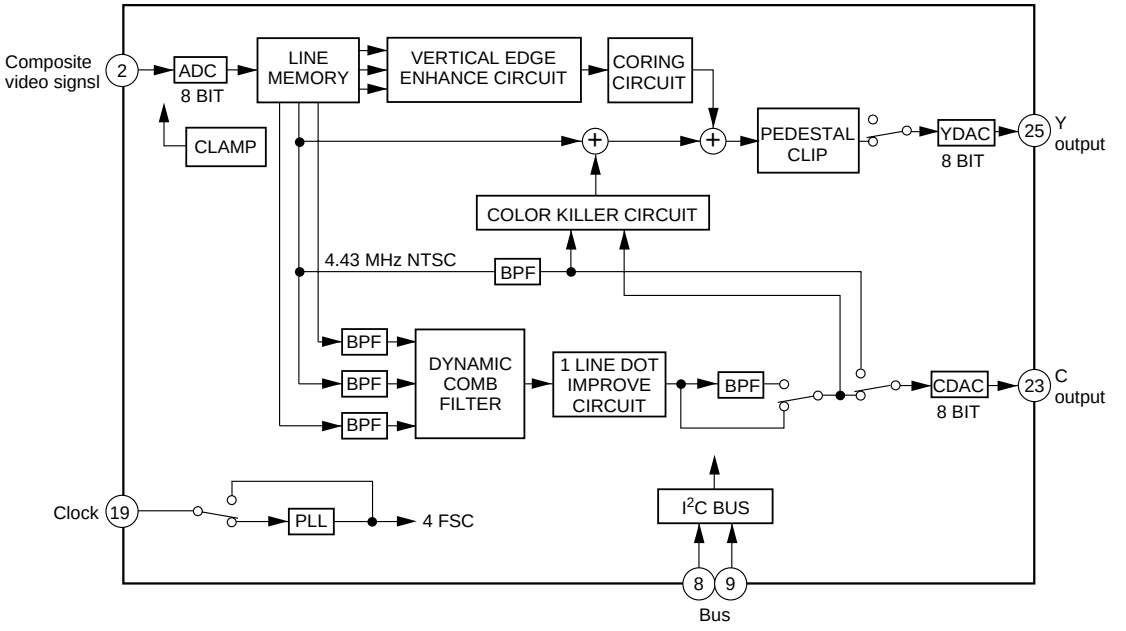


Fig. 7-5 Block diagram of TC9090AN

3-2. Video/Color Circuit

The video/color circuit consists of two ICs, TDA9141 (NTSC/PAL/SECAM DECODER), TDA4665T (BASEBAND DELAY LINE), and supports each system of NTSC, PAL and SECAM.

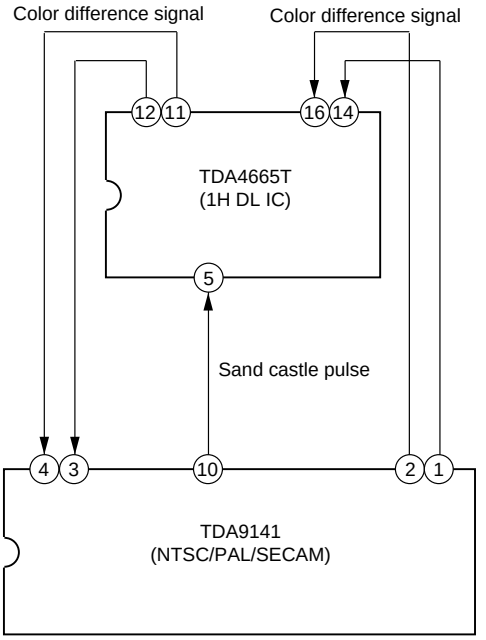


Fig. 7-6

Fig. 7-7 shows the pin configuration of TDA9141 and Fig. 7-8 shows the block diagram of TDA9141. Fig. 7-9 shows the pin configuration of TDA4665T and Fig. 7-10 shows the block diagram of TDA4665T.

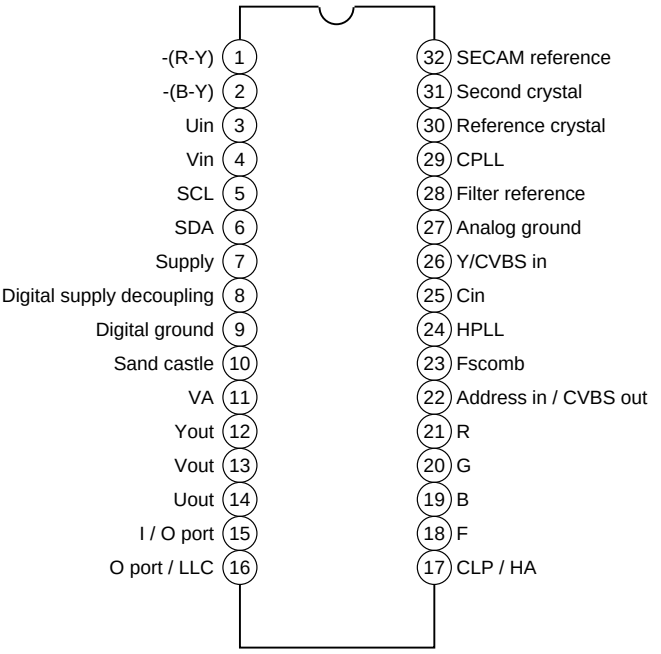


Fig. 7-7 Pin configuration of TDA9141

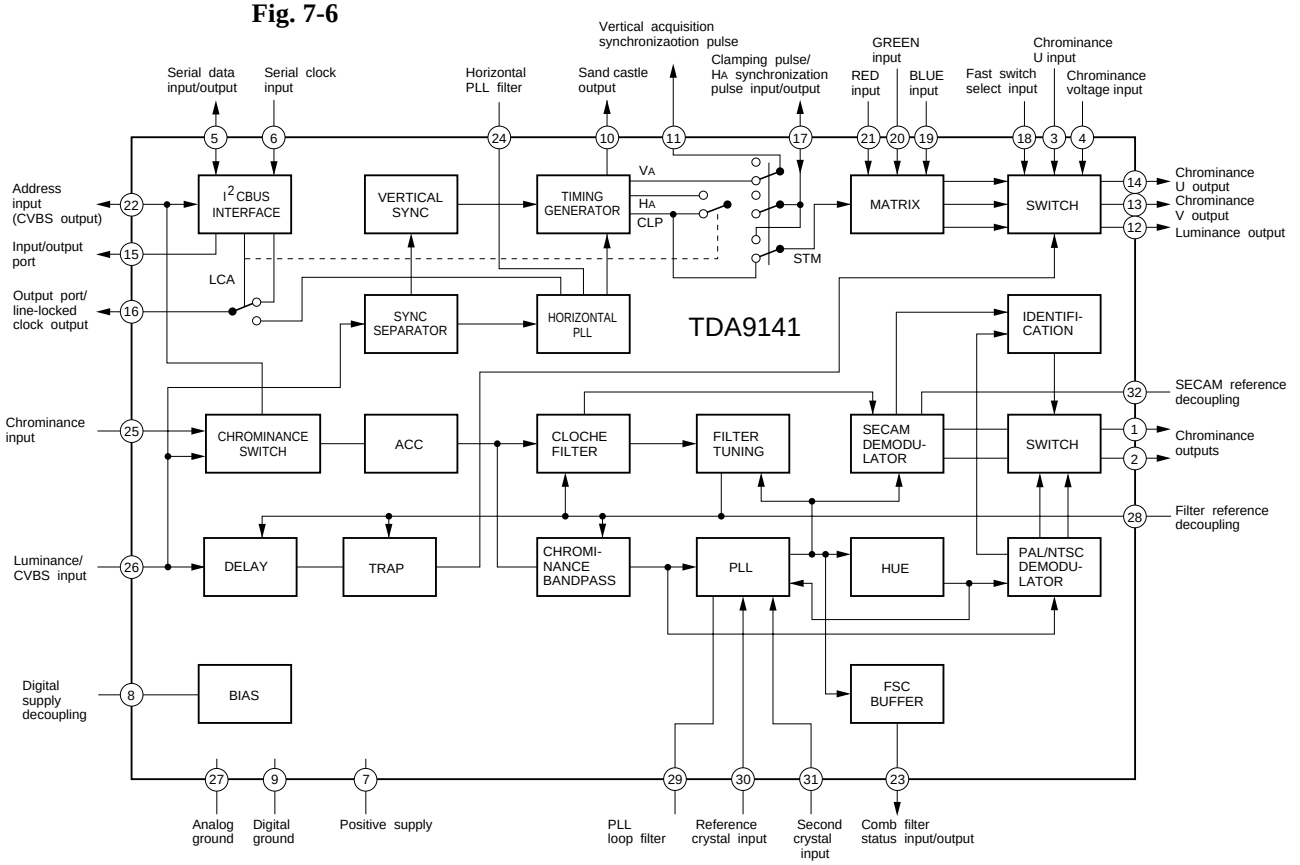


Fig. 7-8 Block diagram of TDA9141

TDA9141 has two input terminals for the composite video/ Y signal (pin 25) and C signal (pin 26), and each of the signals is automatically identified through I²C-BUS control.

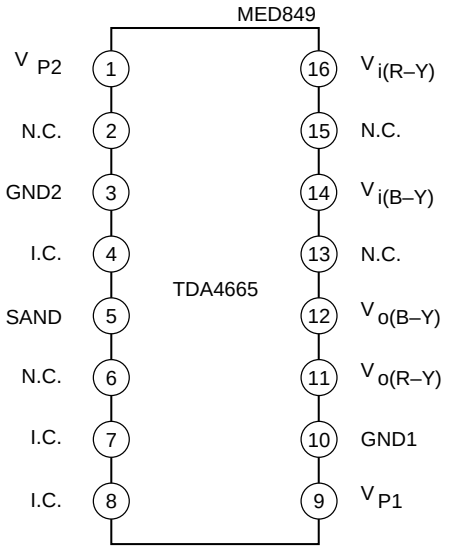


Fig. 7-9 Pin configuration of TDA4665T

Table 7-2 Terminal function of TDA4665T

Pin No.	Name	Function
1	V_{P2}	+5V power supply for digital block
2	N.C.	Not used
3	GND2	GND (0V) for digital block
4	I.C.	Internal connection
5	SAND	Sandcastle pulse input
6	N.C.	Not used
7	I.C.	Internal connection
8	I.C.	Internal connection
9	V_{P1}	+5V power supply for analog block
10	GND1	GND (0V) for analog block
11	$V_{O(R - Y)}$	± (R - Y) output signal
12	$V_{O(B - Y)}$	± (B - Y) output signal
13	N.C.	Not used
14	$V_{i(B - Y)}$	± (B - Y) input signal
15	N.C.	Not used
16	$V_{i(R - Y)}$	± (R - Y) input signal

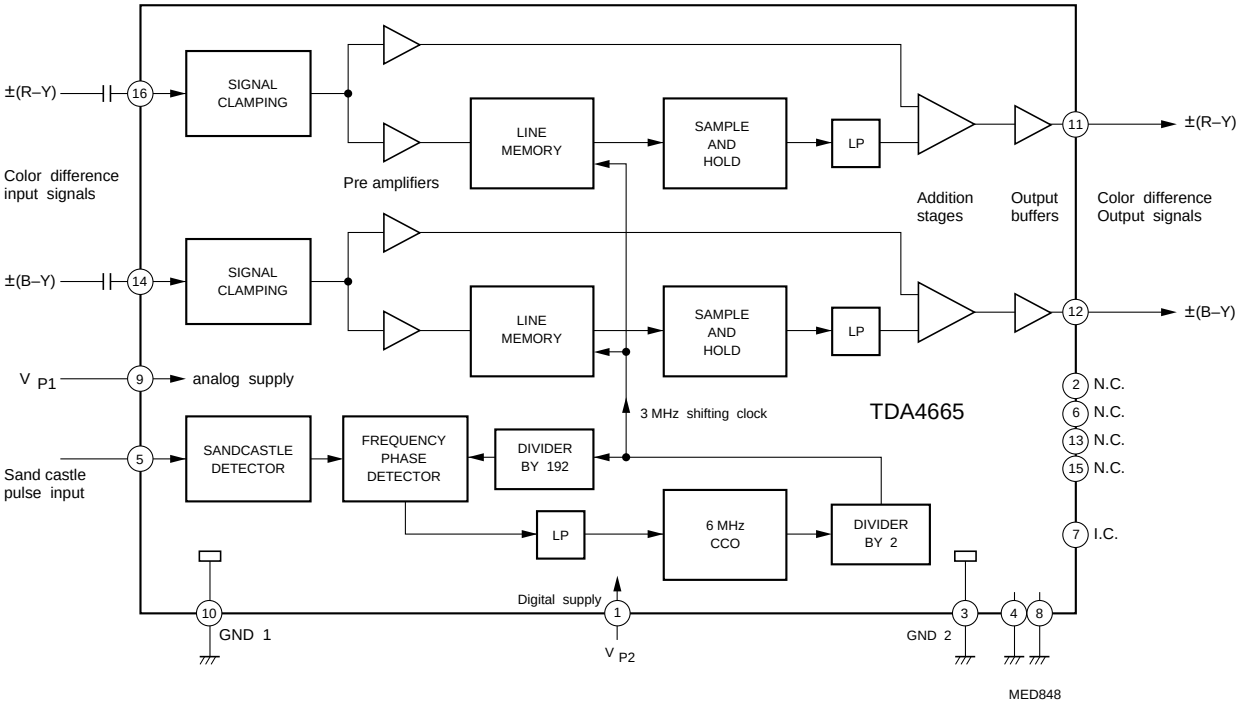


Fig. 7-10 Block diagram of TDA4665T

3-3. Luminance (Y) Signal Process Circuit

The processing method differs as follows depending on type of the signal entered.

(a) For a SECAM input, it passes through a burst signal trap circuit.

(b) For a NTSC/PAL (with burst signal) input (YC separated signals), the burst signal trap circuit is bypassed. It passes through a delay circuit for a phase matching to the color signal.

(c) For a NTSC/PAL (without burst signal) input, above trap circuit and the delay circuit are bypassed to perform a stable color killer operation.

3-4. Color Signal Process Circuit

The color signal is level adjusted in the ACC (automatic color control) circuit, corrected in passing through a band pass circuit in the NTSC/PAL system, or a bell filter correction is carried out in the SECAM system, and then enters the color demodulation circuit.

The input burst signal is locked with a crystal oscillator frequency (3.58 MHz/4.43 MHz) in the PLL circuit and then demodulated into color difference signals after a tint adjustment (in the NTSC system). The demodulation for the SECAM signal is carried out using a PLL circuit.

The demodulated color difference signals are output through low pass filters, delayed by 1H in passing through TDA4665T, fed to TDA9141 again and directly output.

3-5. Picture Sharpness Correction Circuit

The picture sharpness is carried out by TDA4672. Fig. 7-11 shows the pin configuration of TDA4672 and Fig. 7-12 shows the block diagram. The Y signal (luminance signal) enters the IC, and passes through the delay circuit. Amount of the delay can be set to any value between 20ns and 1100ns to the color difference signals.

Picture sharpness correction frequency can be selected either one of 2.6 MHz and 5 MHz. In this unit, the amount of delay is set to 90ns and the picture sharpness correction frequency is set to 2.6 MHz.

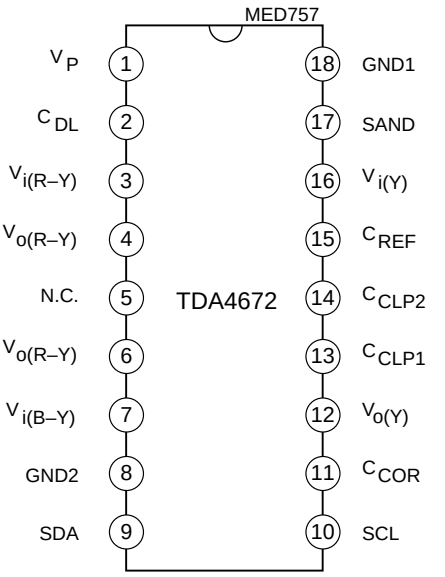


Fig. 7-11 Pin configuration of TDA4672

Table 7-3 Terminal function of TDA4672

Pin No.	Name	Function
1	V_P	Positive power supply
2	C_{DL}	Capacitor for delay time control
3	$V_{i(R - Y)}$	± (R - Y) color difference input signal
4	$V_{O(R - Y)}$	± (R - Y) color difference output signal
5	N.C.	Not used
6	$V_{O(B - Y)}$	± (B - Y) color difference output signal
7	$V_{i(B - Y)}$	± (B - Y) color difference input signal
8	GND2	GND 2 (0V)
9	SDA	I^2C bus data line
10	SCL	I^2C bus clock line
11	C_{COR}	Magnetic core capacitor
12	$V_{O(Y)}$	Delay luminance output signal
13	C_{CLP1}	Black level clamp capacitor 1
14	C_{CLP2}	Black level clamp capacitor 2
15	C_{REF}	Reference voltage capacitor
16	$V_{i(Y)}$	Luminance input signal
17	SAND	Sand castle pulse input
18	GND1	GND 1 (0V)

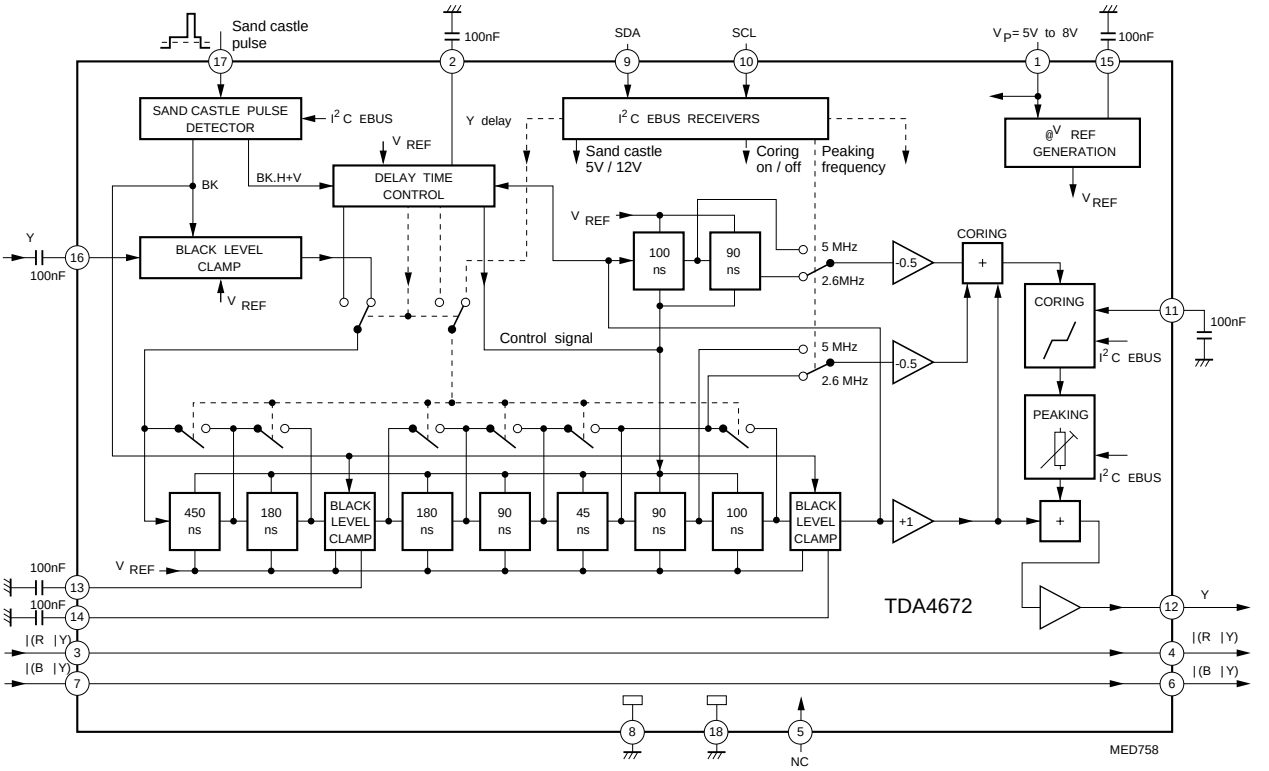


Fig. 7-12 Block diagram of TDA4672

3-6. RGB Demodulation

The demodulation from Y and color difference signals to RGB signals is carried out by TDA4780. Fig. 7-13 shows the pin configuration of TDA4780 and Fig. 7-14 shows the block diagram. The TDA4780 performs the RGB demodulation and adjusts color, contrast, and brightness. The TDA4780 also has functions such as a gamma correction, black extension, blue extension, etc. but they are not used in this unit.

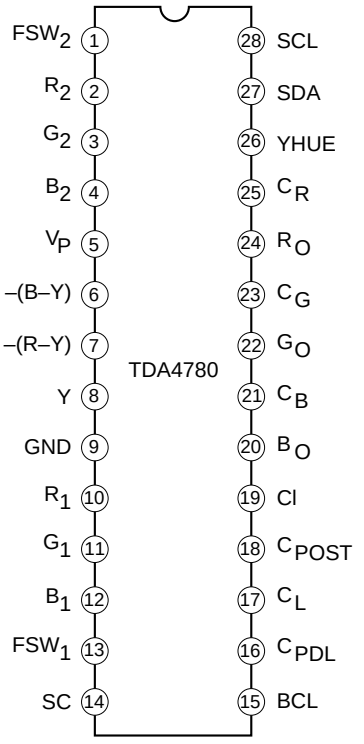


Fig. 7-13 Pin configuration of TDA4780

Table 7-4 Terminal function of TDA4780

Pin No.	Name	Function	Pin No.	Name	Function
1	FSW_2	High speed switch 2 input	15	BCL	Equal beam current limit input
2	R_2	Red input 2	16	C_{PDL}	Memory capacitor for peak limit
3	G_2	Green input 2	17	CL	Memory capacitor for leakage current compensation
4	B_2	Blue input 2	18	C_{POST}	Memory capacitor for peak dark
5	V_P	Power supply voltage	19	CI	Cut-off measurement input
6	- (B - Y)	Color difference input - (B - Y)	20	B_O	Blue input
7	- (R - Y)	Color difference input - (R - Y)	21	C_G	Blue cut-off memory capacitor
8	Y	Luminance input	22	G_O	Green output
9	GND	GND	23	C_G	Green cut-off memory capacitor
10	R_1	Red input 1	24	R_O	Red output
11	G_1	Green input 1	25	C_R	Red cut-off memory capacitor
12	B_1	Blue input 1	26	YHUE	Y output/hue adjustment output
13	FSW_1	High speed switch 1 input	27	SDA	I^2C bus serial data input/check output
14	SC	Sandcastle pulse input	28	SCL	I^2C bus serial clock input

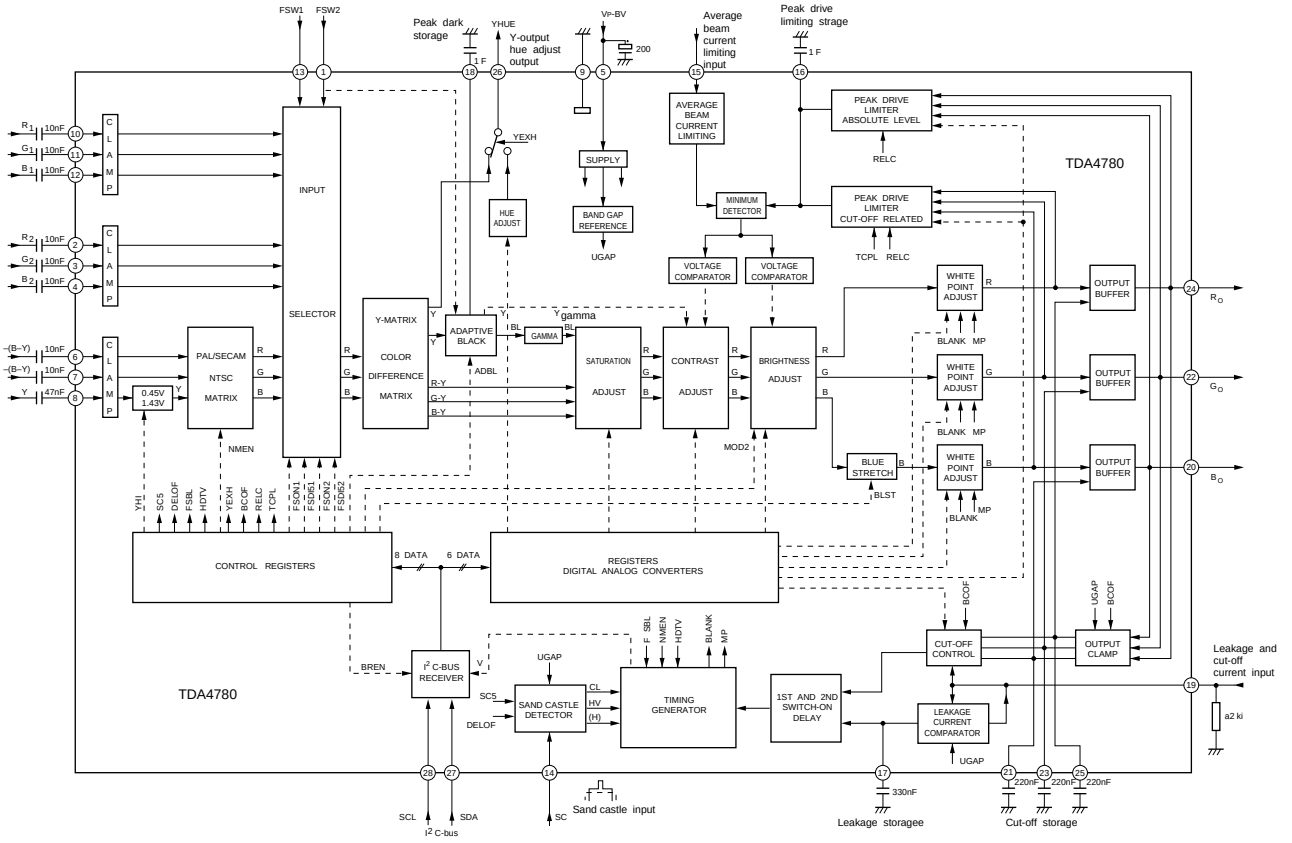


Fig. 7-14 Block diagram of TDA4780

3-7. Audio Circuit

Fig. 7-15 shows the audio circuit block diagram.

Signal path from the Q200 to the LINE OUT terminal is: Q200 Æ transistor buffer Æ LINE OUT terminal.

Signal path from the Q200 to the speaker is as follows. The audio signal output from the Q200 becomes one signal with its L and R signal components mixed. The mixed audio signal entersa the electrical volume IC QA03 (M5222FP) and the output level is controlled within a range of about 0 dB to –80 dB by an external DC voltage (DAC). The audio signal thus controlled by teh IC QA03 is fed to the speaker amplifier IC QA04 (TDA7056A) and amplified by about 36 dB to drive the speaker.

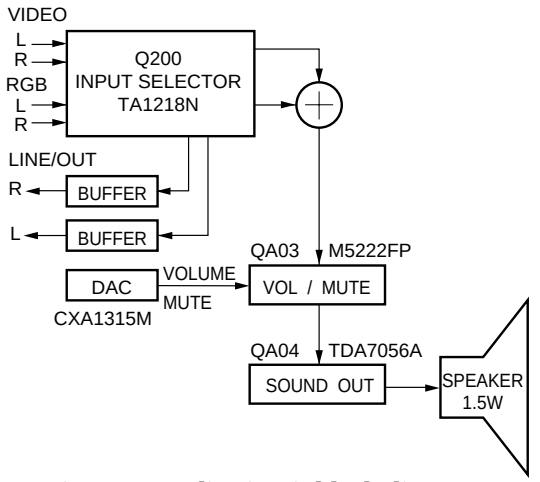


Fig. 7-15 Audio circuit block diagram

4. RGB SIGNAL PROCESS CIRCUIT

4-1. RGB Signal SW Section

The RGB signals are entered from a high density D-SUB 15 pin. The signals are divided into two systems through buffers, the one is input to RGB/video SW section and the other is output from RGB output terminal after the signal is amplified by 6 dB (75W drive) for RGB outputs.

The RGB output signals are always developed as long as signals are being supplied to the RGB input terminal.

The sync signal is corresponding to HD, VD, CS (composite sync) and SYNC ON G. The HD, VD, CS are connected to the sync separation IC Q537 (M52346SP) through a buffer Q512 (74HCT240AF) and RGB output terminals. Sync separation priority is HD, VD, CS, and SYNC ON G in this order.

The HD, VD sync-separated are switched with the HD and VD of the video signal and the switch Q224 (MC14053BF). The falling & rising edges are stabilized by use of AND gates Q225 and Q226 (TC7S08F) in a Schmitt configuration.

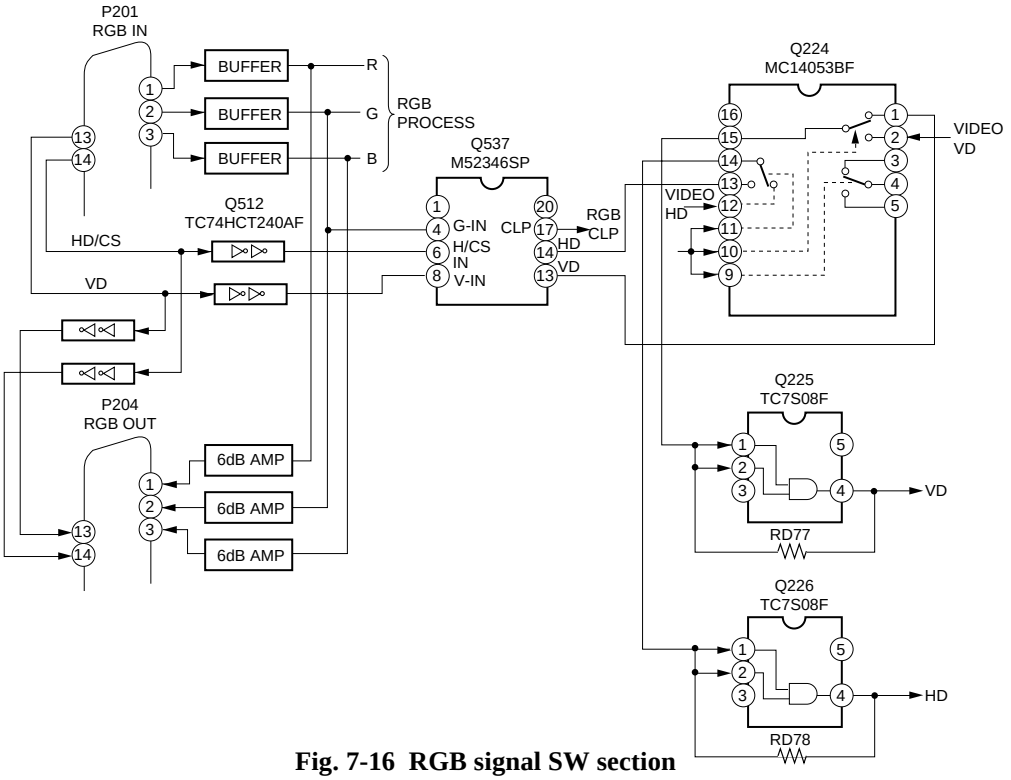


Fig. 7-16 RGB signal SW section

4-2. Video/RGB Signal SW Section

Fig. 7-17 shows a block diagram of the video/RGB SW section. The video signal demodulated in R, G and B signals and the RGB signals input from D-SUB 15P are switched by each analog switch for RGB. The R signal is switched by Q530 (µPD74HC4066A), G signal is by Q525 (µPD74HC4066A) and B signal is by Q520 (µPD74 HC4066A). The switching control is carried out by DAC SW signal and the logic is shown below.

Table 7-5

	µPD74HC4066A	
	Pin 5	Pin 6
Video input	LOW	HIGH
RGB input	HIGH	LOW

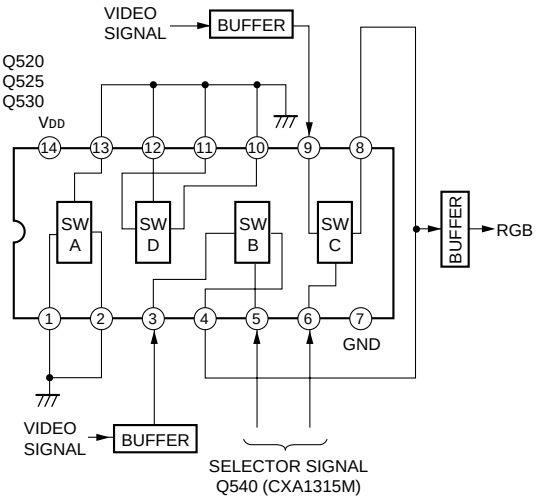


Fig 7-17

4-3. RGB Signal Amplifier Section

The RGB signal processing section employs a wide band RGB signal IC applicable to the SVGA signal. Fig. 7-17 shows a block diagram of Q535 (M52320SP). In this section, OSD mixing is also carried out in addition to the signal amplification.

The control items of the IC are five items; main contrast, sub contrast for each RGB and brightness. The actual control is carried out by using DAC. The main OSD adjustment and sub OSD adjustment are fixed.

The brightness and main contrast controls are provided for the user adjustment, and the sub contrast for RGB is used to adjust the input level of the LCD drive circuit.

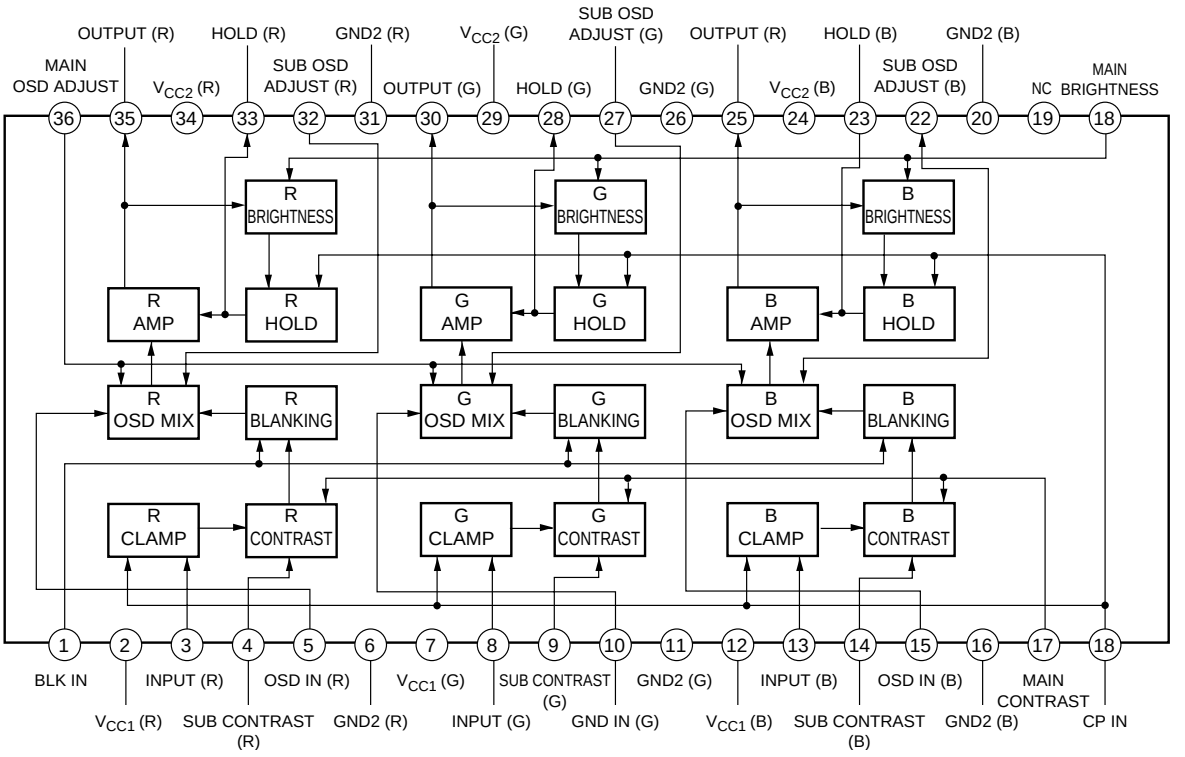


Fig. 7-18

4-4. Microcomputer Interface

Fig. 7-19 shows a block diagram of the peripheral circuit of microcomputer interface circuit. Each kind of control such as signal SW, etc. is carried out by DAC Q540 (CSA1315M) which in turn controlled by I^2C bus for the microcomputer.

The main functions are control of the RGB signal process IC and each kind of signal switching. The sync signal presence/absence at RGB signal input and polarity information are entered from the sync separation IC Q537 (M52346SP) to the I/O port of Q543 (CXA1315), converted into I^2C format, and then sent to the microcomputer.

The logic on the sync signal presence/absence and polarity information is shown in tables 7-6 and 7-7.

Table 7-6 Q540 (CXA1315M)

Pin 3	R sub contrast
Pin 4	G sub contrast
Pin 5	B sub contrast
Pin 6	Main contrast
Pin 7	Brightness
Pin 1	RGB/Video SW control signal
Pin 2	RGB/Video SW control signal
Pin 9	RGB/Video sync SW control signal

	Pin 2	Pin 1	Pin 9
Video input	1	0	0
RGB input	0	1	1

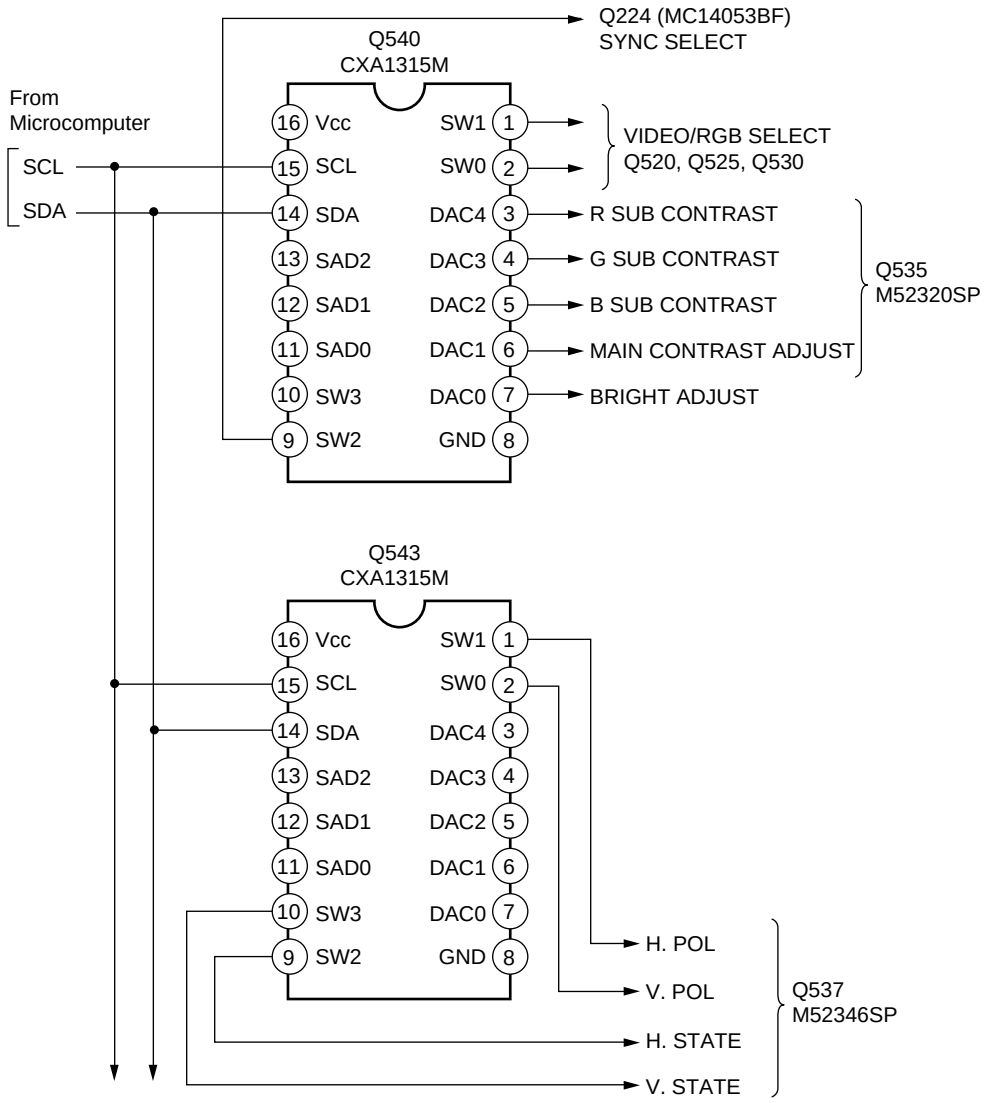


Fig. 7-19

Table 7-7

Q537 (M52346SP) Input status		Q543 (CXA1315)			
Pin 6: HD. COMP	Pin 8: VD	SW0 (#2)	SW1 (#1)	SW2 (#9)	SW3 (#0)
HD. COMP. (POS.)	NON	H	H	L	H
HD. COMP. (POS.)	VD (POS.)	H	H	L	L
HD. COMP. (POS.)	VD (NEG.)	L	H	L	L
HD. COMP. (NEG.)	NON	H	L	L	H
HD. COMP. (NEG.)	VD (POS.)	H	L	L	L
HD.HD. COMP. (NEG.)	VD (NEG.)	L	L	L	L
NON	NON	H	H	H	H
NON	VD (POS.)	H	H	H	L
NON	VD (NEG.)	L	H	H	L
Q537 (M53346SP) output terminal		V. POL (#19)	H. POL (#18)	H. STATE (#1)	V. STATE (#2)

Note:

- The status is inverted as the asctual M52346SP output terminal.

  The logic shown in the tables shows the DAC (CXA1315M) input terminal status.

SECTION VIII
CCD CAMERA CIRCUIT

1. OUTLINE

The camera section of the unit employs the color board camera with 3 times zoom lens. The camera video circuit is assembled in one PC board and composed of the CCD and drive/sync signal generation circuit (SG), pre-amp circuit (CDS), video signal process circuit (PRO, ENC, AWB) and power supply circuit (POW).

Fig. 8-1 shwos a block diagram of CCD camera circuit.

1-1. CCD and Drive/Sync Signal Generation Circuit (SG)

The CCD (QJ01) circuit employs 1/2 inch 410,000 pixels IT-CCD. The horizontal transmission pulse (H1, H2, RG) and vertical transmission pulse (øV1 – øV4, SUB) are supplied through the drive signal generation IC (QJ03) and vertical drive IC (QJ02) by 28 MHz (8 fsc) clock signal output from the oscillator (ZJ01).

Also, the circuit generates a sync signal required for the signal process circuit by inputting the 14 MHz clock signal divided in two at QJ03 to the sync signal generation IC (QJ05).

1-2. Pre-amp Circuit (CDS)

The video signal output from CCD (QJ01) enters the pre-amp IC (QJ04) through the buffer (QJ03). After the signal is processed the noise reduction process (CDS) inside the IC and amplified (AGC), the signal is separated in the luminance signal (YH) and color signals (S1, S2), and then output.

The iris control signal for a lens is supplied to the iris circuit through the buffer (QJ05).

1-3. Video Signal Process Circuit (PRO, ENC, AWB)

The luminance signal (YH) enters the process IC (QL02) through LPF (ZL01, ZL02). After the gamma process is carried out, the signal enters the encoder IC (QL03) through 1H delay IC (QL04).

In the encoder IC (QL03), the horizontal contour signal generated in DL (ZL04) and the vertical contour signal sent from the process IC (QL02) are mixed with luminance signal, and added to the sync signal. The mixed signal is output as a Y signal through 75W driver (QL08).

The color signal (S1, S2) also enters the process IC (QL02) in the same way as the luminance signal.

The color difference signal (R – Y, B – Y) is generated by operating the color signal with the signal through 1H delay IC (QL01), and sent to the encoder IC (QL03) and automatic white IC (QM01) through the vertical corelation noise reduction circuit (the peripheral circuit around QL05 and QL06).

Next, the signal is orthogonal-demodulated with 3.58 MHz (fsc) signal inside the encoder IC (QL03) and then output as a C signal through 75W driver. (QL08).

In the automatic white circuit, the color difference signal (R – Y, B – Y) is input to the automatic white IC (QM01) through the buffer (QM11) and the signal area corresponding to the color temperature variation is extracted inside the IC, thereby creating control signals to set R – Y = 0 and B – Y = 0. Thus obtained signals are sent to the R and B gain control circuits inside the process IC (QL02) through the buffer (QM02).

1-4. Power Supply Circuit

The power supply circuit generates three kinds of DC voltage (+19V, +5V and –9V) necessary to the camera signal process. +5V is output from the switching IC (QK01) of the step down circuit and +19V and –9V are output from the constant voltage circuit (QK05 – QK08) through QK02 –QK04 of the charge pump circuit.

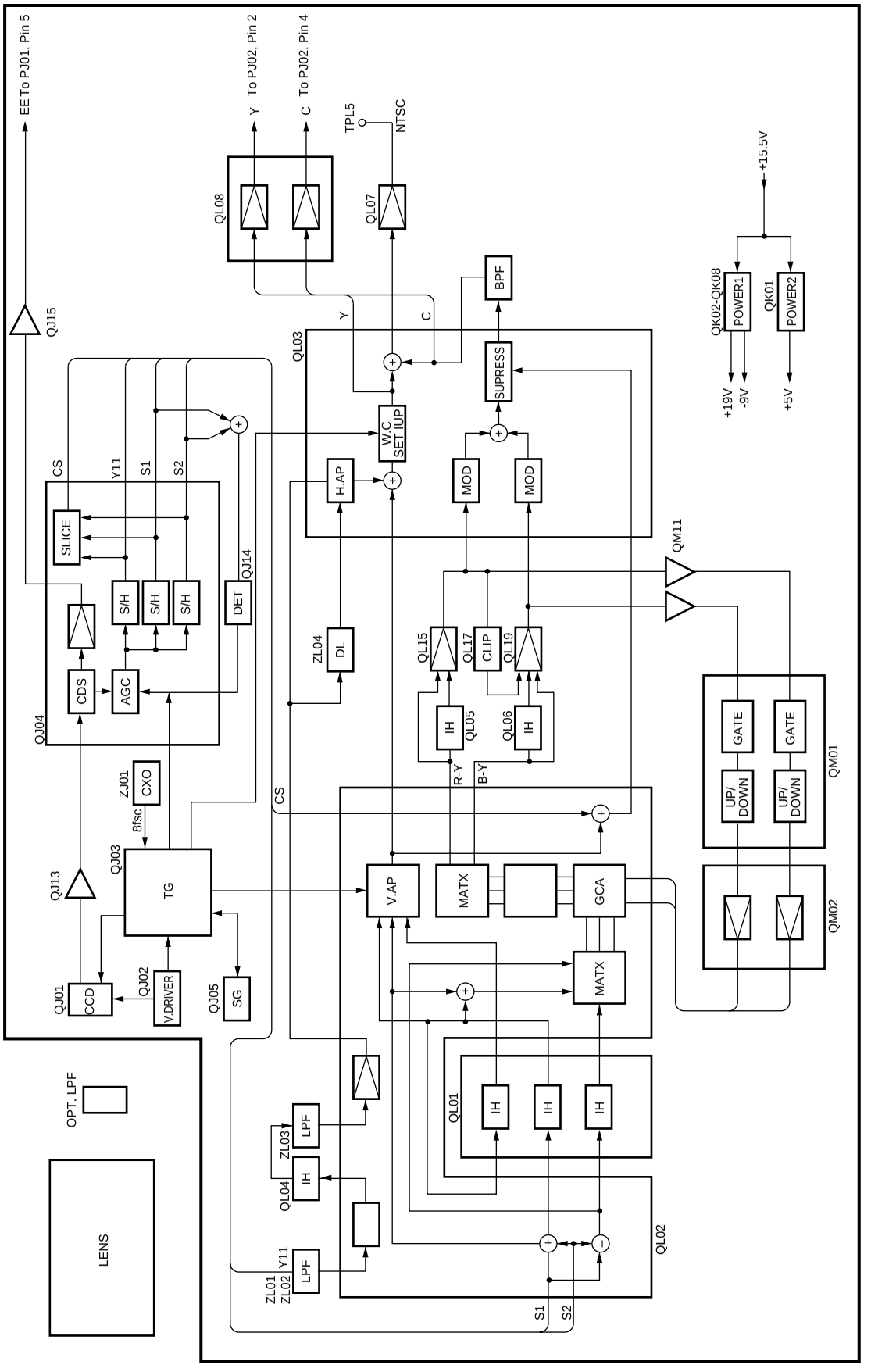


Fig. 8-1 CCD camera circuit block diagram

SECTION IX
FLUORESCENT LAMP INVERTER CIRCUIT

1. OPERATING DESCRIPTION

The base current at start-up passes through QM02, RM04 – RM06 and then flows into the base of QM03. QM02 works as the ON/OFF switch for start-up operation and turns ON when the base voltage develops “L”.

When the base voltage develops “H” (12V), QM02 turns off and QM03 oscillation stops. A current flows into QM01 and RM03 only when the start-up operation is carried out, thus improves the start-up characteristics by increasing the base current of QM03. Especially, this circuit takes effective under the low temperature status where the start-up operation is likely to difficult.

DM03, DM05 and DM06 connected to QM03 base works to prevent cause of an inverse break down overvoltage at QM03 V_{BE}. DM05 and DM06 are connected in series to prevent the overheat at short-circuiting.

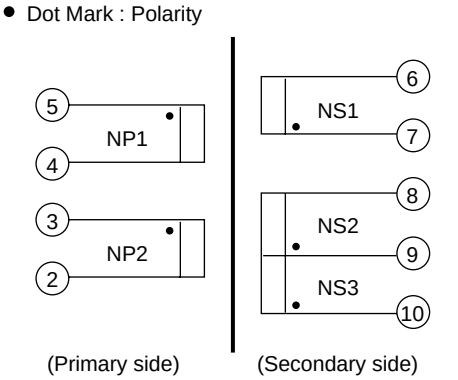
When the resistor value of RM02 is small, heat generation of QM03 lowers. However, if the value is too small, the current of DM03, DM05 and DM06 in continuity becomes large.

DM04 increases only the base current of QM03 when it turns on and reduces the V_{CD} (sat) of QM03 to lower the heat generation. RM07 works as the current limitation resistor of DM04.

CM05 prevents a rapid increase of the collector current of QM03 before the fluorescent lamp turns on.

Also, RM04 is a protective posistor to prevent QM03 from generating temperature more than 120°C.

The specification of LM03 is shown in Figs 9-1, 9-2 and table 9-1.



No.	Coil	Terminal	Turns	Wire	Winding method
1	NP1	5 - 4	24	UEW 0.3	FIT
2	NP2	3 - 2	4	UEW 0.2	SPACE
3	NP2	9 - 8	144	UEW 0.2	FIT
4	NP3	10 - 9	10	UEW 0.2	FIT
5	NP1	7 - 6	10	UEW 0.2	FIT

Fig. 9-2 Winding specification

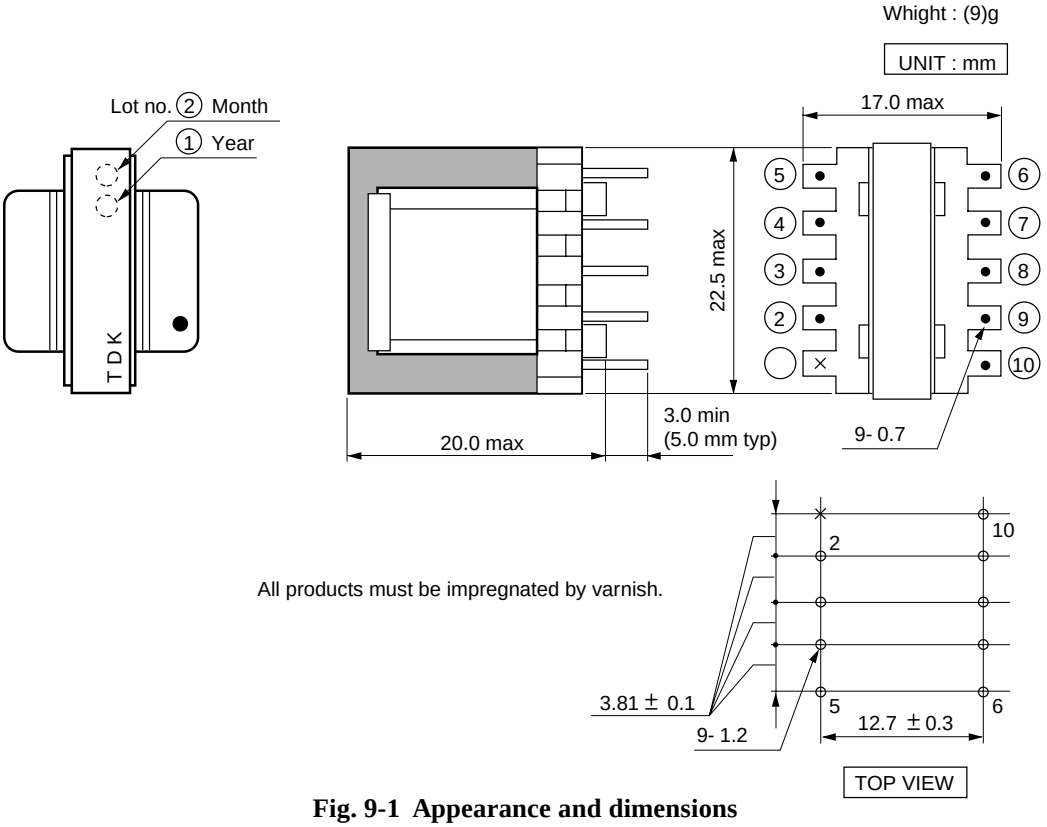


Fig. 9-1 Appearance and dimensions

CM04 is a capacitor to stabilize the fluorescent lamp discharging current. After the discharging starts, CM04 limits the flow of the current with the reactance of CM04 (XC = 1/wc).

Before the fluorescent lamp turns on, the collector pulse of QM03 is 70 – 80 V(p-p). The voltage is stepped up to 420 – 480 V(p-p) by LM03 and applied to the fluorescent lamp. When a filament is warmed, the discharging starts and the collector voltage of QM03 becomes approx. 30 V(p-p). The fluorescent tube voltage at turning on is approx. 120 V(p-p).

SM01 works as a ON/OFF switch for the camera power supply. When pin 10 of SM01 develops "L", the power is supplied to the camera.

The waveforms of each section at operation is shown in Figs. 9-3 and 9-4.

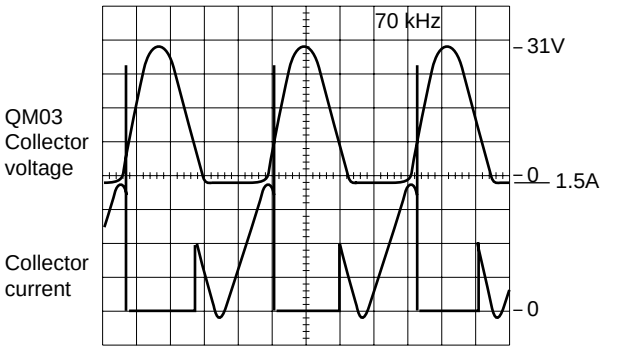


Fig. 9-3

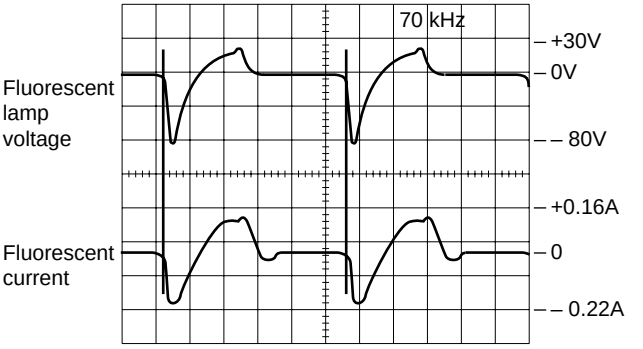
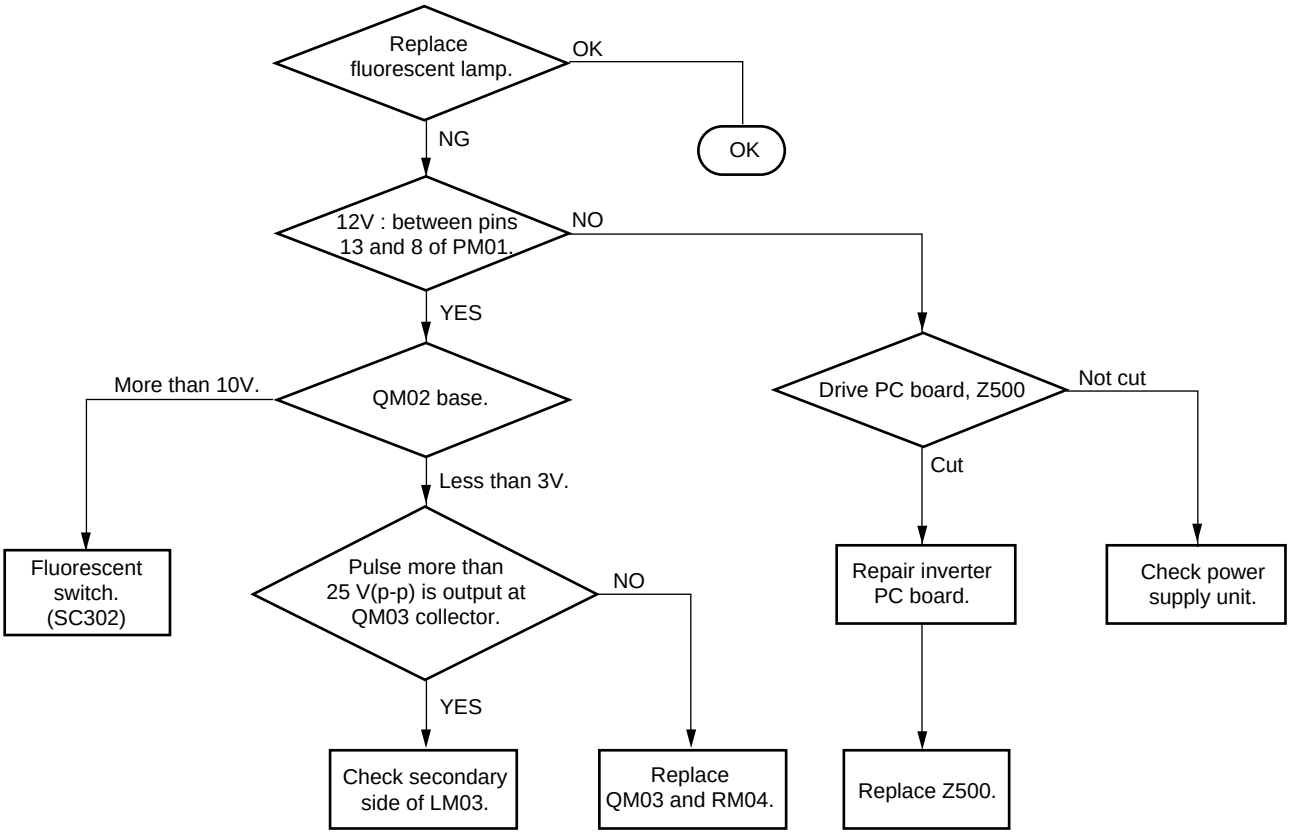


Fig. 9-4

2. TROUBLESHOOTING

2-1. Fluorescent does not turn on



3. CIRCUIT DIAGRAM

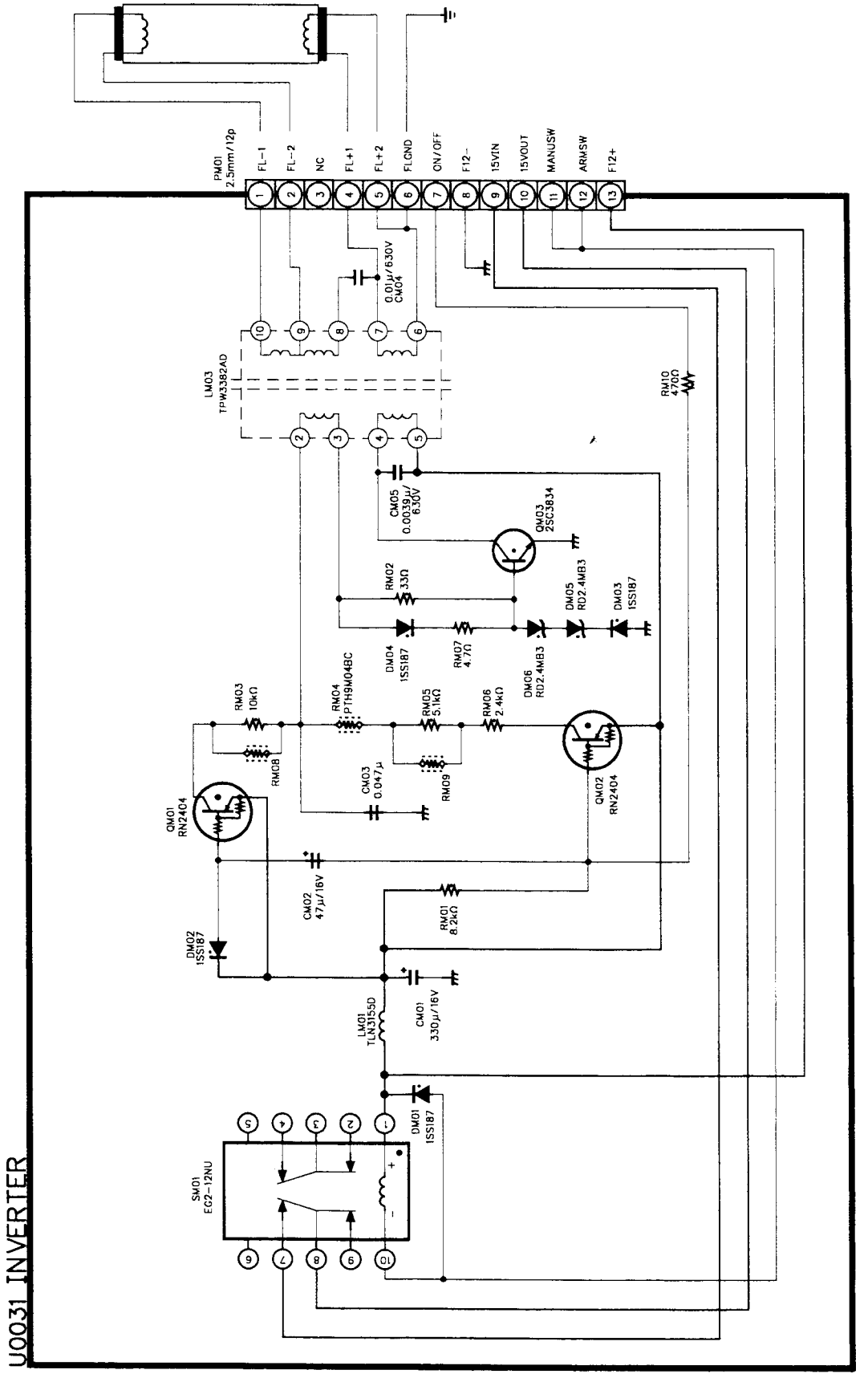


Fig. 9-5 Cicuit diagram

TOSHIBA AMERICA CONSUMER PRODUCTS, INC.
NATIONAL SERVICE DIVISION
1420-B TOSHIBA DRIVE
LEBANON, TENNESSEE 37087