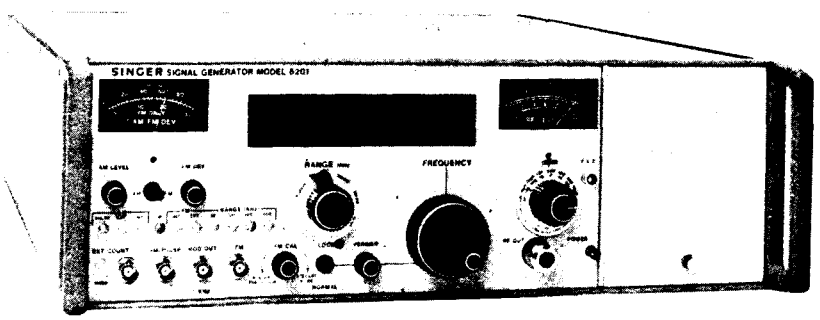
# INSTRUCTION MANUAL

## SIGNAL GENERATOR

### MODEL 6201

### INSTRUCTION MANUAL NO. 110-5103




**SINGER**
**INSTRUMENTATION**

The Singer Company, Palo Alto Operation

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# MANUAL CHANGES

FOR

6201

Make changes and additions as indicated below:

CHANGE 1: Schematic 106-0808-001 and Parts List, Assembly A3A1;

A. Change the value of C22 from .0047 μF to "FACTORY SELECT".

B. Change the value of C16 from 100 pF to 30 pF, ±2%, 500 V, 150-2002-300EGO, 72136, DM15E300GO.

CHANGE 2: Schematic 106-0808-001 and Parts List, Assembly A3A2A1;

A. Change the Singer Parts No. of L4 from 132-0380-001 to 132-0380-004.

B. Change the Singer Parts Nos. of Q1, Q2 from 153-3032-001 to 153-3032-002.

CHANGE 3: Schematic 106-0788-001 and Parts List, Assembly A4A1;

A. Add C76, 1 pF, ±0.1 pF, 50 V, fixed cer., 150-7002-003, 29990, 100-A-1R0-B-C-50.

B. Add R43, 15 Ω, ±10%, 0.10 W, fixed cer., 151-6000-150, 14298, CRC-20-15Ω.

C. On schematic, connect C76, 1 pF to conector of Q7, in series with R48, 15 Ω, to ground.

D. On schematic, change Q7 from RE3754 to D5E.

These changes do not apply to all units, but the D5E transistor requires addition of C76 and R43.

CHANGE 4: Schematic 106-0784-001 and Parts List, Assembly A7;

A. Change the value of R24 from 31.6 KΩ to 21.5 KΩ, ±1%, 1/4 W, fixed MF, 59-21.5K, 19701, MF5C-D-2152F.

B. Delete * from R89 and R59.

C. Add * to R33.

D. Change the value of R59 from 38.3 KΩ to 34.8 KΩ (FACTORY SELECT).

E. Add (FACTORY SELECT) after the value of R33.

F. Change R89 from "FACTORY SELECT" to 20.0 KΩ (FACTORY SELECT).

G. For schematic in upper right hand corner change Pin 5 to read Pin 6. Put wire shielding symbols on wire leading to Pin 9, Pin 8 and Pin 6.

CHANGE 5: Schematic 106-0773-001 and Parts List, Assembly A8A3A6;

A. Change the value of R26 from 560 Ω to 1 KΩ, 151-1002-102J, 19701, CR25-1-4-5P-1K.

B. Change the value of C16 from .01 μF, 150 V to .01 μF, 50 V, 12-88, 8121-100-W5R-103K.

CHANGE 6: Schematic 106-0789-001 and Parts List, Assembly A9A1; change the true mfg. part no. from W005 to 1N4005.

CHANGE 7: Schematic 106-0792-001 and Parts List, Assembly A9A2;

A. Change the Singers Part No. of A9A2 from 103-3028-004 to 103-3028-001.

B. Change Singers Part No. for CR1 from 154-2002-001 to 81-269.

C. Change Singers Part No. for Q11 from 153-3028-001 to 81-140.

D. Change the value of R15, R20 from 1.0 Ω to 0.5 Ω, ±5%, 2.5 W, 151-2029-001, 91637, RS2C-.5Ω-5%.

E. Change the value of R27 from .36 Ω to 0.17 Ω, ±5%, 5 W, 151-2029-001, 91637, RS-5-.17Ω-5%.

Apply part list changes to schematic.

CHANGE 8: Schematic 106-0853-001 and Part List, Assembly A7A2; change Pin J-P1 Meter Ckt (30%) to (15%) and Terminal M-P1 from $\overline{k_1 k_2}$ to $\overline{k_1 \overline{k_2}}$.

CHANGE 9: Schematic 106-0809-001 and Parts List, Assembly A13; change one word from "Remote" to "Operate" at terminal R.

ECO #15161, #15186, #15205, #15214, #15215, #15217, #15220, #15237, #15263.

April 5, 1974

TABLE 1-1. SPECIFICATIONS

| Parameter | Specification |
|---|---|
| **FREQUENCY CHARACTERISTICS** | |
| Frequency Range: | 7.75 - 512 MHz in six bands:<br>Band 1: 248 MHz - 512 MHz<br>Band 2: 124 MHz - 256 MHz<br>Band 3: 62 MHz - 128 MHz<br>Band 4: 31 MHz - 64 MHz<br>Band 5: 15.5 MHz - 32 MHz<br>Band 6: 7.75 MHz - 16 MHz |
| Frequency Vernier Range: | > 300 ppm |
| Frequency Resolution: | Continuously tunable. Six digit frequency display with a least significant digit of 100 Hz (7.75 - 62 MHz) or 1 kHz (62 - 512 MHz). |
| Frequency Accuracy: | |
| Locked mode: | ±(0.05 of last digit + time base accuracy). |
| Unlocked mode: | ±(last digit + time base accuracy). |
| Time Base Accuracy: | |
| Standard: | < ±1 ppm after two hour warm up @ 25°C. |
| Option: | < ±0.1 ppm after two hour warm up @ 25°C. |
| Frequency Stability: | Locked / Unlocked |
| Time (after two hr. warm up): | < 1 ppm/24 hrs. / < 10 ppm/10 mins. |
| Temperature (0°C to 55°C): | <0.33 ppm/°C (Option: 0.03 ppm/°C) / < 60 ppm/°C |
| Line Voltage (±10% change): | < 1 ppm / < 10 ppm |
| Load (open to short): | None / None |
| Level change: | |
| 10 dB vernier | None / 1 ppm |
| 10 dB steps | None / None |
| Mode change: | |
| CW to AM | None / None |
| CW to FM | * / < 150 ppm of carrier frequency |
| Frequency lock hold range: | ±600 ppm or ±10°C min. |
| **SPECTRAL PURITY CHARACTERISTICS** | |
| Residual FM: | |

| Mode | CW | | FM Up to max. Pk. Dev. | |
|---|---|---|---|---|
| Post Detection Bandwidth | 300 Hz - 3 kHz | 20 Hz - 15 kHz | 300 Hz - 3 kHz | 20 Hz - 15 kHz |
| 248 - 512 MHz | < 5 Hz | < 15 Hz | < 9 Hz | < 30 Hz |
| 124 - 256 MHz | < 3 Hz | < 7 Hz | < 5 Hz | < 15 Hz |
| 7.75 - 126 MHz | < 2 Hz | < 5 Hz | < 3 Hz | < 8 Hz |

* Not discernible at modulation frequency $\geq$ 1 kHz, increasing to < 1% peak deviation at 100 Hz modulation frequency.

TABLE 1-1. SPECIFICATIONS (CONTINUED)

| Parameter | Specification |
|---|---|
| **SPECTRAL PURITY CHARACTERISTICS** (Continued) | |
| Spurious Signals: | |
| Harmonics: | > 30 dB below carrier |
| Sub-Harmonics: | > 45 dB below carrier |
| Non-Harmonics: | Not perceptible |
| Broadband Noise: | 130 dB below carrier in a 1 Hz bandwidth at maximum power level vernier position over entire frequency range. |
| **RF POWER OUTPUT CHARACTERISTICS** | |
| Output Power Control Range: | 20 dBm (2.2 V) to -146 dBm (0.01 μV) in 10 dB steps with continuous adjustment between steps. Output level indicated on attenuator and meter calibrated in dBm and volts into nominal 50 Ω load. |
| RF Output Level Accuracy: | |
| Output Level Range: | +20 dBm to -10 dBm / -10 dBm to -50 dBm / -50 dBm to -146 dBm |
| Total inaccuracy as indicated on output meter and step attenuator (including flatness, calib. inaccuracy, attenuator inaccuracy, meter linearity, detector response, etc.) | Up to 125 MHz ±1.0 dB / Up to 125 MHz ±1.5 dB / Up to 125 MHz ±2.2dB<br>Up to 512 MHz ±1.2 dB / Up to 512 MHz ±1.8 dB / Up to 512 MHz ±2.5 dB |
| Auxiliary Accuracy Specifications: | |
| Attenuator Accuracy: | ±0.15 dB/10 dB cumulative. Up to ±1.5 dB max. |
| RF Level Flatness: | Up to 125 MHz: ±0.25 dB<br>Up to 512 MHz: ±0.5 dB |
| Meter Linearity: | ±2% of full scale. |
| Output Impedance: | 50 Ω nominal. |
| Output VSWR | < 1.25 @ ≤ 0 dBm; <1.5 @ > 0 dBm |
| Output Connector: | Type N Female. |
| **MODULATION CHARACTERISTICS** | |
| Internal AM: | |
| Frequency: | 1 kHz screw driver adjustable ±2% (rear panel). |
| Range: | Zero to 100% indicated on AM meter calibrated in % modulation. |
| Accuracy of Indicated AM: | ±8% of reading (20% - 100%) over top 3 dB of vernier range.<br>±16% of reading (20% - 100%) over remaining 7 dB of vernier range. |
| Incidental FM - Up to 125 MHz: (30% AM) | < 150 Hz peak |
| Up to 512 MHz: | < 300 Hz peak |
| AM Distortion: (over top 3 dB of vernier range) | < 5% up to 70% AM fc < 250 MHz<br>< 3% up to 30% AM fc > 250 MHz<br>< 10% up to 70% AM fc > 250 MHz |

# SECTION III
# THEORY OF OPERATION

## 3–1. SIMPLIFIED BLOCK DIAGRAM DESCRIPTION.

3-2. The Signal Generator is basically a master/oscillator/power amplifier, with additional frequency divider, modulator, counter/stabilizer, and modulation selection circuits. Figure 3-1 functionally illustrates the Signal Generator in simplified form, ignoring the physical location of its circuits in respect to the assemblies on which the circuits are mounted. Important switches and controls are included to familiarize the user with the function of each.

3-3. The master oscillator is a UHF cavity oscillator that is tunable from 248 to 512 MHz. For all frequency ranges except the highest range (248 - 512 MHz), the oscillator output is divided by a high-speed binary frequency divider, providing six one-octave tuning bands from 7.75 to 512 MHz for the Signal Generator. The master oscillator has applied either a DC to 200 kHz signal for frequency modulation, or a DC voltage for fine frequency tuning.

3-4. The frequency divider output is fed to a balanced modulator for level control (automatic and manual) and amplitude or pulse modulation (when selected) of the RF output. The insertion loss of the balanced modulator can be manually varied over a range of about 16 dB by an adjustable RF level set control in the output of the modulator selection circuit. The modulator output is then coupled to the wideband power amplitude.

3-5. The power amplifier boosts the low level signal from the modulator up to 100 milliwatts maximum (+20 dBm) into 50 ohms. Following the power amplifier, lowpass filters selected by the frequency RANGE MHz control attenuate frequency divider harmonics, and any power amplifier distortion products. A succeeding 150 dB step attenuator operates in conjunction with the adjustable RF level set control to provide a total amplitude range of 166 dB for the Signal Generator output.

3-6. The RF output level is kept flat across the entire frequency range, independent of band switching, by the automatic level control feedback loop. In this feedback loop, the RF output level is detected, and returned to a level control amplifier that continuously compares the output of the detector to a DC reference voltage obtained from the RF level set controls (output of amplitude modulation circuit). The resultant control amplifier output automatically adjusts the insertion loss of the balanced modulator so that the RF level at the detector is kept constant at any level from +4 to +20 dBm. The loop virtually eliminates variations in the RF output level due to changes in master oscillator output level, frequency divider output level, broadband power amplifier gain and other frequency dependent sources of amplitude variation within the loop. The RF detector output is also coupled to the RF LEVEL meter, which indicates the RF output level in conjunction with the attenuator.

3-7. The modulation capabilities of the Signal Generator include AM, FM and pulse, with negligible interaction when using two modes concurrently (i.e., AM/FM or FM/pulse). When AM operation is selected, the modulation selection and AM/FM metering circuitry injects either an internally-generated 1 kHz signal or an external DC to 100 kHz into the automatic level control feedback loop of the balanced modulator and level control circuitry. The percentage of modulation, which is variable from zero to 100 percent, is indicated on the % AM/FM DEV meter (when selected by the AM/FM switch). When FM operation is selected, either the aforementioned internally generated 1 kHz signal or an external DC to 200 kHz signal is applied to a varactor within the master oscillator cavity structure. Since the FM signal path is direct-coupled, the center frequency, as well as the deviation, can be controlled over a narrow band by the external voltage coupled to the FM connector. The FM peak deviation, which is variable from zero to 1000 kHz, is indicated on the % AM/FM DEV meter (when selected by the AM/FM switch). Pulse modulation is obtained by coupling the external modulating signal at the AM/PULSE connector to the extremely linear and broadband balanced modulator. A sample and hold circuit within the modulator maintains the automatic level control feature operative during pulsed operation.

3-8. The output frequency of the Signal Generator is digitally indicated by a six decade counter which is driven by the lowest output frequency (7.75 - 16 MHz) of the frequency divider. The counter gate interval is automatically programmed by the setting of the RANGE MHz switch to indicate the actual output frequency on six LED (Light Emitting Diode), 7-segment displays. An external signal between 100 Hz and 10 MHz can also be measured by the frequency counter without interrupting normal operation of the Signal Generator.

3-9. The frequency lock circuitry operates in conjunction with the frequency counter. During frequency lock operation, the normal count sequence is interrupted, and the last count is fixed on the LED display. The counter and lock circuits then lock the master oscillator frequency to the frequency indicated on the display. The lock output voltage is fed back to the master oscillator to compensate for frequency drift. In unlocked mode, the VERNIER frequency control output is applied through the lock output circuit for fine frequency tuning. The frequency lock circuit is disabled whenever the counter is used for external count.

3-10. The band center command circuitry generates command level and command pulse outputs from the lowest output frequency of the frequency divider. The band center command level is applied to the frequency divider and low-pass filter circuits to cause filter switching in these circuits to occur near the geometric center (355 MHz) of the master oscillator frequency tuning range; and the band center command pulse is fed to the balanced modulator to blank the Signal Generator output during the band center low-pass filter transition.

3-11. The regulated power supplies convert a 115 or 230 VAC, 47 to 420 Hz power input to five regulated DC outputs (+5, +6, +12, -5.2 and -26 VDC).

## 3-12. DETAILED BLOCK DIAGRAM DESCRIPTION.

3-13. The following paragraphs describe the operation of the functional blocks of the Signal Generator on a detailed block diagram level. For detailed circuit descriptions of the functional blocks, refer to Section IV of this manual.

**NOTE**

Unless otherwise indicated in any of the logic circuit discussions, a logical ZERO level is 0 volts DC (nominal) and a logical ONE level is +5 volts DC (nominal).

3-14. FREQUENCY GENERATION CIRCUITRY.

3-15. This circuitry consists of the 248 - 512 MHz master oscillator and the frequency divider. The circuitry, which is contained on assemblies A1 and A2, is shown in Figure 3-2 and described in the following subparagraphs.

3-16. 248 - 512 MHz Master Oscillator. The basic 248 to 512 MHz sinusoidal waveform employed to develop all lower signal frequencies is generated by tunable master oscillator A1. The oscillator comprises a UHF power transistor (A1A1Q1) which is coupled to a tunable 1/4 wavelength resonant coaxial cavity. Rotation of the FREQUENCY control mechanically moves a ceramic slug to change the physical length of the cavity, thereby tuning the master oscillator. A varactor diode in the cavity has applied one of the following inputs from the modulation selection and AM/FM metering circuitry (paragraph 3-38): a DC to 200 kHz signal for frequency mdoulation; or a vernier/AFC DC voltage for fine frequency tuning over a range of at least 300 ppm. Output power is extracted by loop coupling at the shorted end of the coaxial cavity.

3-17. Frequency Divider. Two buffer amplifiers (A2A1Q1/Q5 and A2A1Q2) are provided at the input of the frequency divider chain to provide isolation from the master oscillator. The 248 - 512 MHz output of buffer amplifier A2A1Q1/Q5 is applied to the frequency divider chain and the 248 - 512 MHz output of buffer amplifier A2A1Q2 is applied to the RANGE MHz selector. The frequency divider chain is composed of a 5-stage high-speed binary divider. The divider stages are connected in cascade. Each stage has a binary divider (A2A2A1Q1/Q2, A2A2A2Q1/Q2, A2A2A3MC1, A2A3A1MC1, or A2A3A2MC1) and a buffer amplifier (A2A2A1Q3/Q4, A2A2A2Q3/Q4, A2A2A3Q1, A2A3A1Q1 or A2A3A2Q1) for isolation from the succeeding binary divider. The output of each binary divider is applied to a buffer amplifier and to the RANGE MHz selector. The divided output selected by the RANGE MHz selector is applied to the balanced modulator and level control circuitry (paragraph 3-19). The 7.75 - 16 MHz output from divider A2A3A2MC1 is applied (via buffer amplifier A2A3A2Q1) to the frequency counter circuitry (paragraph 3-55) and to the band center command circuitry (paragraph 3-52).

3-18. Two low-pass filters (A2A2A1C1-C3, A2A2A1L1 and A2A2A1CR1; and A2A2A2C1-C3, A2A2A2L1, and A2A2A2CR1) with switchable upper cutoff frequencies are provided in the frequency divider chain. When the output frequency of the master oscillator is below the geometric mean of its range (355 MHz), the band center command input (0 volts) causes the cut off frequency of the filters to be just above the geometric mean of the band. This action causes the filters to attenuate unwanted harmonic products of the divided signals from A2A2A1Q1 and A2A2A2Q1, thereby providing a clean sinusoidal output to drive the modulator. Similarly, when the output frequency of the master oscillator is above the geometric mean, the band center command input (+5 volts) causes the cutoff frequency of the filters to be shifted slightly above the high end of the band, while maintaining a steep skirt. This action again provides a clean output waveform for driving the modulator.

3-19. BALANCED MODULATOR AND LEVEL CONTROL CIRCUITRY.

3-20. This circuitry is principally composed of a wideband preamplifier, two balanced modulators in series, an RF level control circuit, and a sample and hold circuit. The circuitry, which is mostly contained on assembly A3, is shown in Figure 3-3 and described in the following paragraphs.

3-21. Wideband Preamplifier. The 7.75 to 512 MHz signal output from the frequency generation circuitry (paragraph 3-14) is applied to a two-stage wideband preamplifier consisting of RF amplifiers A3A2A1Q1 and A3A2A1Q2. The gain of the preamplifier (which employs degenerative feedback from Q2 to Q1) is approximately 15 dB from 5 to 550 MHz; its output power level is approximately 1 milliwatt (0 dBm).

3-22. Balanced Modulators. The amplified 7.75 to 512 MHz RF output from the wideband preamplifier is applied to first balanced modulator A3A2A2. During the various modes of operation, the insertion loss of this modulator and second balanced modulator A3A2A3 is varied to affect the preamplifier output as follows. In CW, pulsed or FM operation, the DC correction voltage output of the RF level control circuit (paragraph 3-23) varies the RF impedance of the diodes within the balanced modulators to offset any variation in the RF output of the Signal Generator. An AC signal is superimposed on the DC voltage in AM operation, thereby causing amplitude modulation of the preamplifier RF output to be achieved at the balanced modulators. When in pulsed operation, the pulse command (+12 volts DC) from the modulation selection and AM/FM metering circuitry (paragraph 3-38) provides $+V_{cc}$ for inverter A3A1Q1 and initially cuts off the diodes of the balanced modulators, via gates A3A1Q13 and A3A1Q14 and emitter followers A3A1Q12 and A3A1Q15. The external pulse signal from the modulation selection and AM/FM metering circuitry (which is applied through inverter A3A1Q1 and the aforementioned gates and emitter followers to the balanced modulators) then causes the modulator diodes to pass the wideband preamplifier output with minimum loss for the duration of each applied pulse. During band center switching, the balanced modulators are turned off by the blanking pulse from the band center circuitry (paragraph 3-52) in an identical manner as described above for the pulse command.

3-23. RF Level Control Circuit. This circuit consists of RF detector A5A1A1A1 leveling amplifier A3A1MC2, isolation amplifier A3A1Q11, and emitter followers A3A1Q12 and A3A1Q15. A DC reference voltage from the modulation selection and AM/FM metering circuitry (paragraph 3-38) is applied to the inverting input of the leveling amplifier, when in CW, FM or pulsed operation. Also applied to the inverting input of this amplifier (and the RF level meter) is a portion of the RF output at the low-pass filter circuitry (paragraph 3-29), via the RF detector (and the sample and hold circuit when in pulsed

operation). The resulting error (sum) voltage is then amplified and inverted by the leveling amplifier, and coupled through isolation amplifier A3A1Q11 and emitter followers A3A1Q12 and A3A1Q15 to the first and second balanced modulators. Thus, the operating point of the diodes within the balanced modulators is adjusted so that the RF output level remains constant independent of the signal frequency.

3-24. When the Signal Generator is set for AM operation, the leveling amplifier input from the modulation selection and AM/FM metering circuitry consists of the DC reference voltage with superimposed AC. This input results in amplitude modulation of the RF signal at the balanced modulators via the RF level control circuit. During pulsed operation, the +12 volts DC pulse command from the modulation selection and AM/FM metering circuitry gates FET switch A3A1Q10 (via switches A3A1Q7 through Q9). Under this condition, resistor A3A1R35 is bridged across the existing feedback network (A3A1R32 and A3A1C7) of the leveling amplifier, thereby reducing its DC gain.

3-25. The RF LEVEL meter derives its voltage from the summing circuit described in paragraph 3-23. With the VX2 pushbutton in the released position, the meter circuit consists of potentiometer A7R22 in series with RF LEVEL meter M2. Under this condition, the RF LEVEL meter is calibrated to read full scale for +14 dBm at the output of the RF detector. When the VX2 pushbutton is pressed, the following three things occur: +12 volts is switched to the level set network of the modulation selection and AM/FM metering circuitry, thereby increasing the RF output voltage by a factor of 2 and changing the calibration of the RF meter circuit; potentiometer A7R23 is placed is series with A7R22 to compensate for the increased RF output so that meter M2 reads full scale with +20 dBm; and +12 volts is applied to the VX2 indicator, causing it to light.

3-26. Sample and Hold Circuit. This circuit consists of inverters A3A1Q2, A3A1Q4, and A3A1Q5; FET switch A3A1Q6; and unity-gain amplifier A3A1MC1. When in pulsed operation, the external pulse signal coupled to the PULSE/AM connector is applied to inverter A3A1Q2, via the modulation selection and AM/FM metering circuitry (paragraph 3-38). Modulation pulses in excess of +0.5 volts DC drive A3A1Q2 into saturation for the duration of each applied pulse, gating FET switch A3A1Q6 on (via inverters A3A1Q4 and Q5) and allowing capacitor A3A1C11 to charge to the negative output level of RF detector A5A1A1A1. The RF detector output level stored by the capacitor is then coupled through the high input impedance unity-gain amplifier and the normally closed contacts of de-energized relay A3A1K1 to the RF level control circuitry (paragraph 3-23). The R-C time constant of A3A1R20 and A3A1C11 allows the sample and hold circuit to retain the RF detector output during those periods when the modulating pulse is not present, thereby keeping the succeeding RF leveling loop at an operating point comparable to that for CW operation. During pulsed operation, the +12 volts DC pulse command from the modulation selection and AM/FM metering circuitry keeps relay A3A1K1 in the de-energized condition, via switches A3A1Q7 and A3A1Q8.

3-27. WIDEBAND POWER AMPLIFIER.

3-28. The output of the balanced modulator and level control circuitry is coupled to the wideband power amplifier (Figure 3-4), a seven-stage power amplifier chain having a total gain of approximately 50 dB and a 3 dB bandwidth from below 5 MHz to beyond 530 MHz. The output of the power amplifier is applied to the low-pass filter circuitry.

3-29. LOW-PASS FILTER CIRCUITRY.

3-30. The wideband power amplifier output, which is rich in harmonics due to the characteristics of the signal applied, is coupled to the low-pass filter circuitry (Figure 3-4). This circuitry consists of five electronically actuated reed relays (A5A1K1 through K5), a magnetically actuated reed relay (A5A1K6), relay drivers (A5A1A2Q1 through Q3), and a manually-driven filter selector turret switch (A5A4) containing six pairs of low-pass filters. The turret switch is mechanically ganged to the RANGE MHz selector.

3-31. When the RANGE MHz selector is set to any position other than PLUG-IN, the wideband power amplifier output is applied simultaneously to reed relays A5A1K1 and A5A1K3. A band center command voltage, obtained from the band center command circuitry (paragraph 3-53) is applied to switch A5A1A2Q1. When the output frequency of the 248 - 512 MHz master oscillator is below its geometric mean of 355 MHz, the band center command level is 0 volts, causing switches A5A1A2Q1 and A5A1A2Q2 to cut off and switch A5A1A2Q3 to saturate. This, in turn, causes reed relays A5A1K3 and A5A1K4 to energize, thereby inserting the appropriate low end, low-pass filter into the signal path. Each low end filter has an extremely sharp skirt at its high frequency limit to sharply attenuate harmonics of the carrier frequency generated by either the frequency divider, modulator or power amplifier.

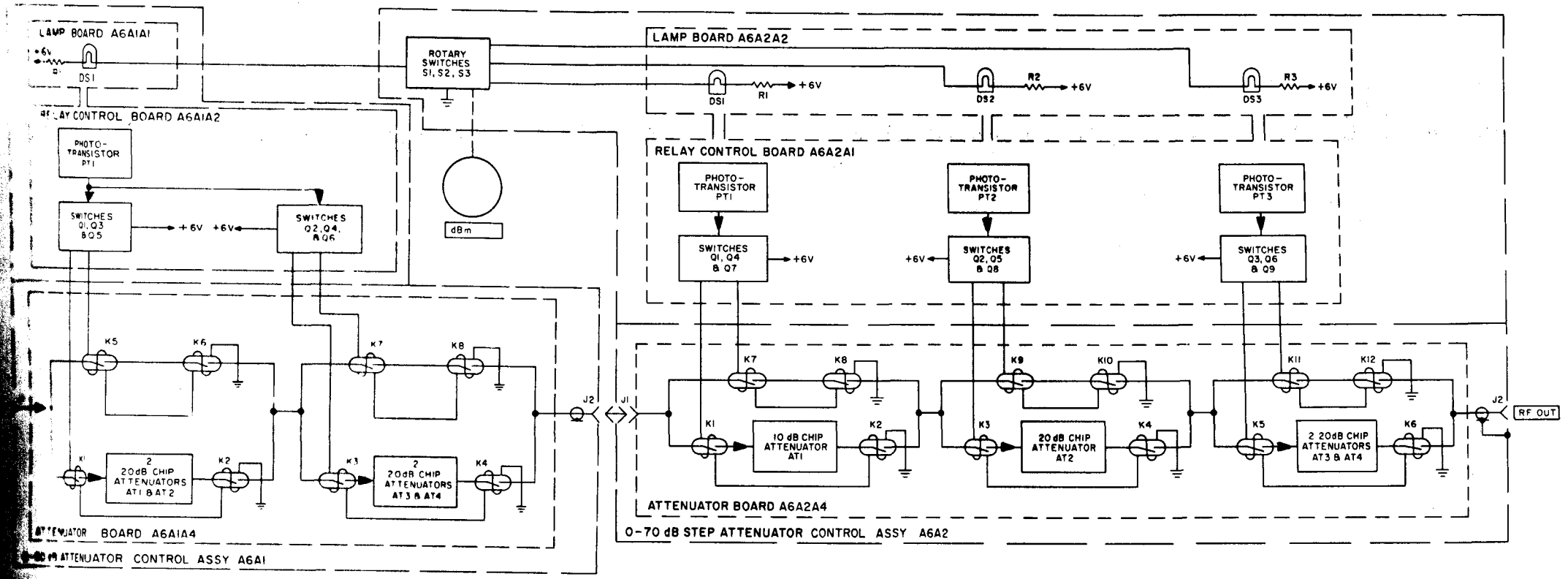
3-32. Similarly, when the output frequency of the master oscillator is above its geometric mean of 355 MHz, the band center command level is +5 volts, causing switches A5A1A2Q1 and A5A1A2Q2 to saturate and switch A5A1A2Q3 to cut off. This, in turn, causes reed relays A5A1K1 and A5A1K2 to energize, thereby inserting the appropriate high end, low-pass filter into the signal path. Each high end filter has an extremely sharp skirt at its high frequency limit to greatly attenuate unwanted harmonics of the carrier frequency.

3-33. The output of the selected low-pass filter (as determined by the setting of the RANGE MHz selector and the operating frequency of the master oscillator) is simultaneously applied to RF level detector A5A1A1A1 and the balanced modulator and level control circuitry (paragraph 3-19); and, through an RC network (A5A1A1R2, A5A1A1C1 and A5A1A1C2) that establishes a 50-ohm output impedance, to the 0 - 150 dB output attenuator circuitry (paragraph 3-35).

3-34. When the RANGE MHz selector is set to the PLUG-IN position, a permanent magnet on the rotor of the turret switch is placed in close proximity to reed relay A5A1K6. Closure of the relay contacts energizes reed relay A5A1K5, thereby allowing the output of the plug-in module (if used) to be coupled to both the RF level detector and the 0 - 150 dB step attenuator circuitry. Resistor A5A1A1R3 establishes the plug-in module output impedance at 50 ohms.

3-35. 0 - 150 dB STEP ATTENUATOR CIRCUITRY.

3-36. The step attenuator circuitry (Figure 3-5) employs two step attenuator assemblies (A6A1 and A6A2) to adjust the RF output level over a 150 dB range, in 10 dB steps.




3-5

Figure 3-5. 0-150 dB Step Attenuator Circuitry, Detailed Block Diagram

One attenuator assembly (A6A2) consists of 10 dB, 20 dB, and 40 dB chip (two 20 dB chips in series) attenuators, which provides up to 70 dB of attenuation in 10 dB steps. The other attenuator assembly (A6A1) contains four 20 dB, a total of 80 dB which is inserted in one step. The desired attenuation, from 0 to 150 dB, is obtained by inserting and bypassing various combinations of the 10, 20, 40 and 80 dB attenuators as indicated in Table 3-1 and described below.

3-37. When the dBm switch is set to +10/1.0V, all attenuators are bypassed. Lamps A6A1A1DS1 and A6A2A2DS1 through DS3 are out since the path to ground through the dBm switch wafers is not completed. Under this condition, examine the state of the 10 dB chip attenuator. Since lamp A6A2A2DS1 is not illuminated, phototransistor A6A2A1PT1 is in cutoff, placing both A6A2A1Q1 and A6A2A1Q4 in saturation and A6A2A1Q7 in cutoff. Saturation of A6A2A1Q4 energizes the coils which activate reed relays A6A2A4K7 and A6A2A4K8 to bypass the 10 dB chip attenuator, while A6A2A1Q7 in cutoff opens reed relays A6A2A4K1 and A6A2A4K2 to open circuit the chip. The same occurs when the dBm switch is set to any odd decade value (e.g., -10, -30, -50, etc.). The opposite results when the dBm switch is set to even decade values (e.g., 0, -20, -40, etc.). Lamp A6A2A2DS1 illuminates, phototransistor A6A2A1PT1 conducts, placing both A6A2A1Q1 and A6A2A1Q4 in cutoff and A6A2A1Q7 in saturation. The 10 dB chip attenuator is then inserted into the RF signal path. The same sequence of events occurs for the 20 dB and 40 dB steps of attenuation. The 80 dB step attenuator is also similar in operation, except that all four 20 dB chips are connected in series by reed relays A6A1A4K1 through K4 or all four are bypassed by reed relays A6A1A4K5 through K8. The reed relays are actuated by parallel switching circuits A6A1A4Q1 through A6. The attenuator output is available at the front panel RF OUT jack.

TABLE 3-1. dBm SWITCH SETTING VS STEP ATTENUATOR INSERTION

| dBm Switch Setting | Attenuation Inserted | | | |
|---|---|---|---|---|
| | 10 dB Chip | 20 dB Chip | 40 dB Chip | 80 dB Chip |
| +10/1.0V | | | | |
| 0/0.3V | X | | | |
| -10/.10V | | X | | |
| -20/.03V | X | X | | |
| -30/10 mV | | | X | |
| -40/3 mV | X | | X | |
| -50/1.0 mV | | X | X | |
| -60/0.3 mV | X | X | X | |
| -70/.10 mV | | | | X |
| -80/.03 mV | X | | | X |
| -90/10 μV | | X | | X |
| -100/3 μV | X | X | | X |
| -110/1.0 μV | | | X | X |
| -120/0.3 μV | X | | X | X |
| -130/.10 μV | | X | X | X |
| -140/.03 μV | X | X | X | X |

3-38. MODULATION SELECTION AND AM/FM METERING CIRCUITRY.

3-39. The modulation selection and AM/FM metering circuitry is mostly contained on assembly A7. The circuitry is shown in Figure 3-6 and described in the following subparagraphs.

3-40. CW Operation. When the front-panel CW pushbutton (A7S4) is pressed, all modulation pushbuttons are released. Under this condition, the internal 1 kHz oscillator (paragraph 3-51) is de-energized and all external modulation signals coupled to the Signal Generator are disconnected by AM PULSE pushbutton A7S1, AM EXT pushbutton A7S2 and FM EXT pushbutton A7S5. In addition, with the AM PULSE pushbutton released, the generation of a pulse command (paragraph 3-42) is inhibited.

3-41. The regulated +12 volts supply output is applied to the RF level set network consisting of resistors A7R3 and A7R1, and dBm vernier control A6A1R1 in parallel with A7R5; this produces a DC reference voltage of approximately +4 volts across A6A1R1 with front-panel VX2 pushbutton S5 in the released position. When the VX2 pusybutton is pressed, switched +12 volts is applied to the junction of A7R3 and A7R1 (effectively bypassing A7R3 in the level set network), thereby increasing the DC reference voltage to approximately +8 volts. The resulting DC reference voltage output from the dBm vernier control varies the insertion loss of the balanced modulators of the balanced modulator and level control circuitry (paragraph 3-19) over a dynamic range of typically 60 dB. When in CW operation, +12 volts is applied to CW indicator A7DS1 (via the released modulation selector pushbuttons), causing it to illuminate.

3-42. Pulsed Operation. When AM PULSE pushbutton A7S1 is pressed (thereby releasing the AM INT and AM EXT pushbuttons), a pulse command (+12 volts) and the external pulse input at AM/PULSE connector J10 are applied to the balanced modulator and level control circuitry (paragraph 3-19). In pulsed operation, the RF level set network operates identically as when in CW operation (paragraph 3-40).

3-43. Amplitude Modulation. When AM EXT pushbutton A7S2 is pressed (thereby releasing the AM PULSE and AM INT pushbuttons), the Signal Generator is set for external AM operation. In this mode of operation, the external AM signal coupled to AM/PULSE connector J10 is applied through AM LEVEL control R1 to both the RF level set network (A7R1, A7R3, A7R5 and A6A1R1) and AM metering buffer amplifier A7Q1. At the level set network, the AM signal is superimposed on the DC reference level; the resulting AM + DC signal is then applied to the balanced modulator and level control circuitry (paragraph 3-19) where actual amplitude modulation is achieved. Note that when in AM operation, the VX2 pushbutton must be in the released position. This limits the maximum unmodulated RF output power level during AM operation to +14 dBm, thereby permitting modulations of up to 100% to be attained at full rated output power (+20 dBm).

3-44. The external AM signal at the output of AM metering buffer amplifier A7Q1 is detected by A7CR1 and the resulting DC signal (which is proportional to the modulating signal level) is routed through % AM calibration screwdriver control A7R14 to AM/FM selector switch S1. When this switch is set to AM, the DC signal is applied to % AM/FM DEV meter M1, where a visual indication of the percentage modulation is presented. Note that, since the modulating signal level is superimposed on the DC reference level, adjustment of dBm vernier control A6A1R1 has no effect on the percentage modulation for a given setting of the AM LEVEL control.

3-45. When AM INT pushbutton A7S3 is pressed (thereby releasing the AM PULSE and AM EXT pushbuttons), the internal 1 kHz oscillator (paragraph 3-51) is energized. The 1 kHz tone is then applied through the AM LEVEL control to the RF level set network and the AM metering buffer amplifier. At this time, any external modulation signal coupled to the AM/PULSE connector is open-circuited.

3-46. Frequency Modulation. When FM EXT pushbutton A7S6 is pressed (thereby releasing the FM INT pushbutton), the Signal Generator is set for external FM operation. The external FM signal at FM connector J12 is coupled through FM DEV R2 and closed contacts 1 and 2 of released FM CAL switch S3 to both stage A7Q3A of an FM amplifier (via FM CAL control R5) and FM metering buffer amplifier A7A4 (via one of six bandswitch attenuator networks). After amplification by A7Q3/Q4 and A7Q6, the external FM signal is applied to the varactor within master oscillator A1. FM DEV control R2 permits adjustment of the frequency deviation obtained by a given modulating signal, while VERNIER frequency control R4 permits fine tuning of the master by adjusting the quiescent DC operating point of A7Q3B, via the frequency lock circuitry (paragraph 3-79). When the FM EXT and FM INT pushbuttons are both released, the external FM signal is disconnected from the master oscillator varactor. Under this condition, only the vernier tuning signal is applied to the master oscillator.

3-47. The six bandswitch attenuator networks at the input of FM metering buffer amplifier A7A4 ensure that the peak deviation indicated on the % AM/FM DEV meter corresponds with the actual deviation of the RF output frequency. In band 1, the FM deviation sensitivity is 0.338 volt/100 kHz peak deviation. The deviation sensitivity decreases by 50% for each successive band (e.g., 0.338 volt/50 kHz peak deviation for band 2, 0.338 volt/25 kHz peak deviation for band 3, etc.). The external FM signal at the output of FM metering buffer amplifier A7A4 is routed through range buffer amplifier A7A5 (via one of four meter multiplier networks), AC detector A7A6, and DC amplifier A7A7 to AM/FM selector switch S1. When this switch is set to FM, the DC output of A7A7 is applied to % AM/FM DEV meter M1, where a visual indication of the deviation sensitivity is presented. Precision resistors A7R15 through R21, in conjunction with FM RANGE (kHz) pushbuttons A7S7 through S10, function as FM meter multipliers.

3-48. Calibration of the deviation sensitivity is accomplished by means of an internal +0.338 volt reference obtained from the +12 volt power supply through the voltage divider consisting of precision resistors A7R79 through R81. When FM CAL pushbutton S3 is pressed, the +0.338 volt reference level is coupled to the FM amplifier in place of the external modulating signal. The desired deviation sensitivity is obtained by initially adjusting FM CAL control R5 from the maximum counterclockwise position until exactly an increase of .100 is observed on the frequency counter display. The FM CAL switch is then placed in the released position and

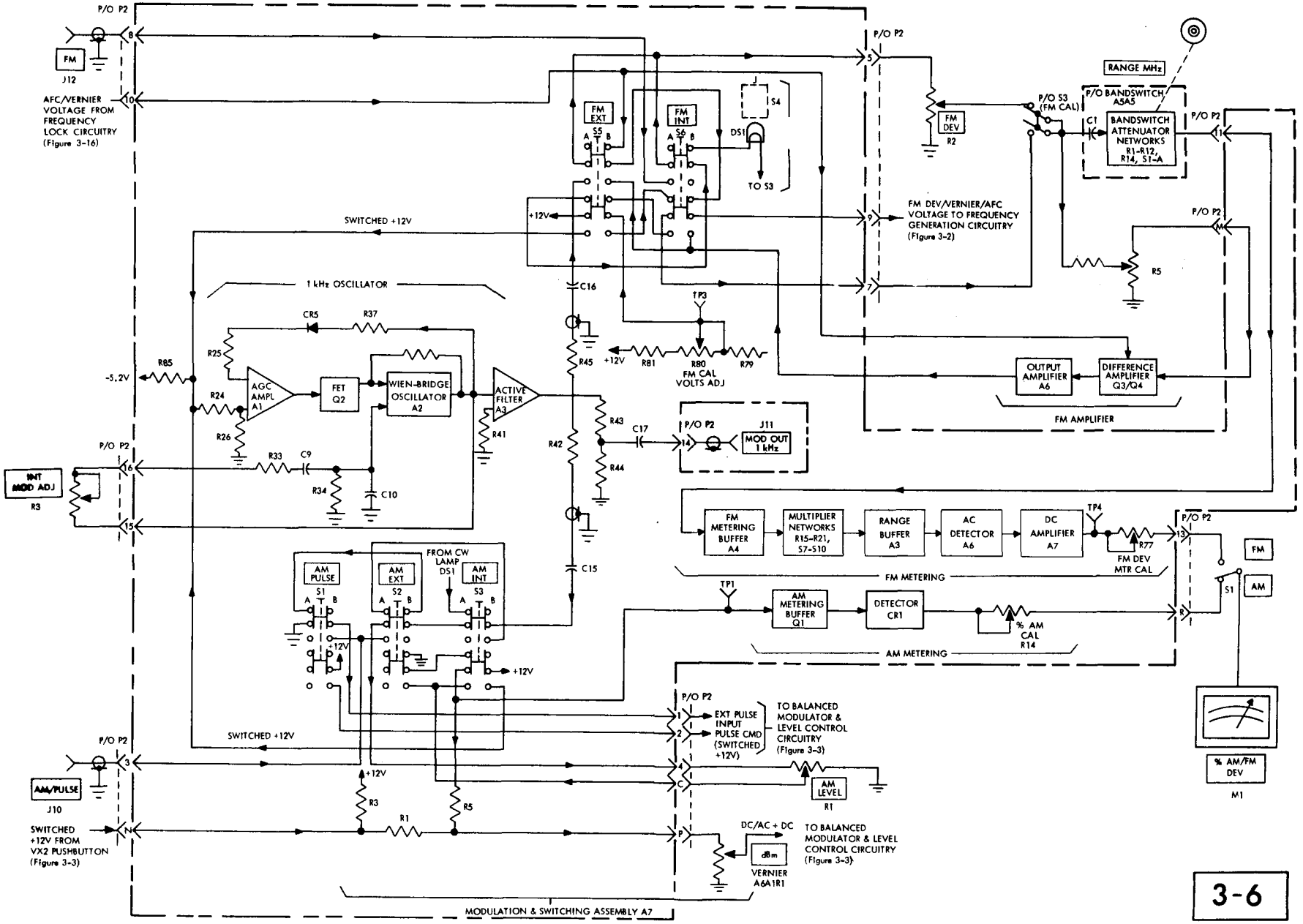



Figure 3-6. Amplitude Modulation, AM Metering and Demodulators Circuitry, Detailed Block Diagram

the FM DEV control is adjusted until the desired sensitivity is observed on the % AM/FM DEV meter.

3-49. As in the case for AM operation, the Signal Generator can be frequency modulated by the internal 1 kHz oscillator (paragraph 3-51). When FM INT pushbutton A7S5 is pressed (thereby releasing the FM EXT pushbutton), the 1 kHz oscillator is energized. The 1 kHz tone is then coupled to the FM DEV control in place of the modulating signal applied to the FM connector.

3-50. Concurrent Modulation. Paragraphs 3-40 through 3-49 detail the operation of each modulation mode. By simply set ing the Signal Generator for simultaneous operation in two independent modes (one being frequency modulation and the other being either amplitude or pulse modulation), concurrent AM/FM or FM/pulse outputs can be obtained.

3-51. Internal 1 kHz Oscillator. A 1 kHz audio signal for internal amplitude modulation or frequency modulation of the RF output is generated by Wien bridge oscillator A7A2, when AM INT pushbutton A7S3 or FM INT pushbutton A7S5 is pressed. When either of these pushbuttons is pressed, +12 volts is applied to AGC amplifier A7A1, causing FET A7Q2 to be gated on. This, in turn, causes the Wien bridge oscillator to be energized. The oscillator output, which may be varied ±2 percent of 1 kHz by rear-panel INT MOD ADJ screwdriver control R3, is coupled through active filter A7A3 (which eliminates any distortion in the oscillator output) to 1 kHz MOD OUTPUT connector J11 and to the AM and/or FM circuits. Any variation in the oscillator output level is sensed by detector A7CR5, amplified by A7A1, and applied to the FET, which acts as a variable resistor to maintain the output level constant.

3-52. BAND CENTER COMMAND CIRCUITRY.

3-53. The 7.75 to 16 MHz output from the final stage of the frequency divider chain (paragraph 3-17) is used by the band center command circuitry (Figure 3-7) to generate the band center command level and pulse signals. The input circuit consists of an amplifier/limiter (A8A3A6Q6, Q5). The output of the amplifier/limiter circuit is coupled to a low-pass filter whose insertion loss is approximately 5 dB at 11.093 MHz. This frequency corresponds to the geometric mean (355 MHz) of the master oscillator tuning range. The low-pass filter output is applied to detector A8A3A6CR1, which is used to drive Schmitt trigger A8A3A6Q1/Q2. Since the detector polarity is negative, the input to the base of A8A3A6Q1 goes positive as frequency increases. The result is that, at the high end of the frequency band, A8A3A6Q1 is saturated and A8A3A6Q2 is cutoff. Potentiometer A8A3A6R1 adjusts the Schmitt trigger hysteresis so that the trigger switches at about 11.1 MHz when tuning up in frequency, and at about 10.9 MHz when tuning down. Potentiometer A8A3A6R2 adjusts the DC bias level on which the detector output rides.

3-54. The output of the Schmitt trigger is fed to two gate circuits (A8A3A6Q3 and Q4), and then to a delay logic circuit (A8A3A6IC1/IC2). The delay logic circuit has two outputs: the first output is the band center command level, which is logical ZERO at the low end of the frequency band, and logical ONE at the high end of the frequency band. The other delay logic output is a positive-going pulse that drives an output monostable multivibrator (A8A3A6IC3). The quiescent output state of the delay logic is logical ZERO; at band center transitions, the output is a positive pulse. The delay logic output pulse then drives the output monostable multivibrator circuit, which generates the band center blanking pulse.

3-55. FREQUENCY COUNTER CIRCUITRY.

3-56. This circuitry, which is contained on assembly A8, performs the following functions: it provides a highly accurate frequency measurement of the Signal Generator output signal or an external signal from 100 Hz to 10 MHz; and it operates in conjunction with the frequency lock circuitry (paragraph 3-79) to give crystal stability of the Signal Generator output signal. The following subparagraphs provide a description of the overall operation of the frequency counter circuitry, and a detailed block diagram description of each of its functional circuits.

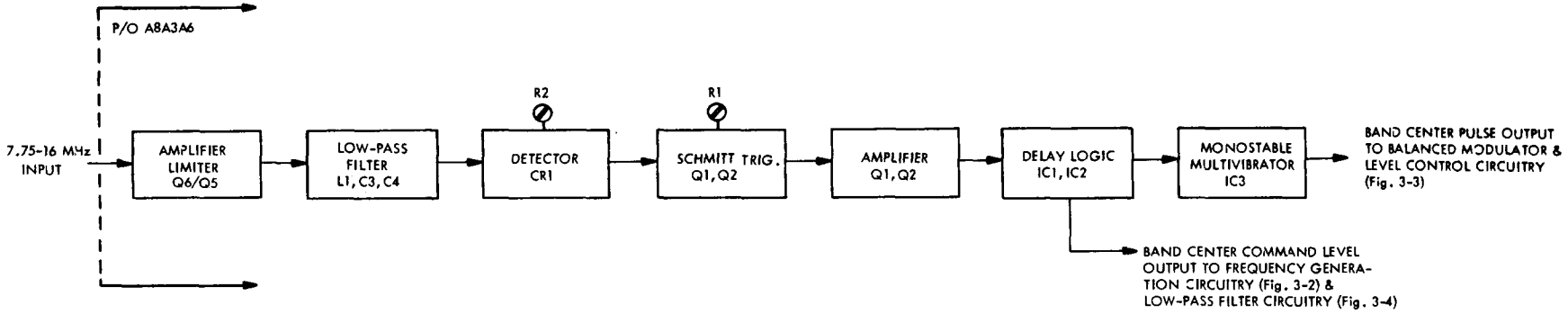
3-57. Counter Overall Operation. In the normal count mode (unlock operation), the counter circuitry counts the number of pulses ($f_c$) that are gated during a selected count interval ($\Delta T$). The count (product of $f_c$ and $\Delta T$) is then stored and displayed directly on a six-digit LED readout, together with the range. During external count operation, a fixed count interval is employed to directly count the applied signal frequency.

3-58. In the frequency lock mode, the count operation is inverted. The counter counts the $f_c$ pulses backward to zero. At the zero count, the counter generates a LOAD command which pre-sets the counter with the stored number and a ZERO pulse that drives the frequency lock circuitry. This circuitry, in turn, compares the timing of the ZERO pulse with the timing of a stable reference signal from the frequency counter circuitry. The resulting DC signal from this comparison is then used to control the frequency of the master oscillator.

3-59. Figure 3-8 is a block diagram of the frequency counter. The 7.75 to 16 MHz output from the frequency divider chain (paragraph 3-17) is used to generate the $f_c$ pulses. The count input is divided by the pre-scaler circuitry, which has five division ratios: 2 (for frequency lock), 8, 16, 32 and 64. The correct sub-harmonic is selected by the $f_c$ gate commands from the control logic circuitry, which is controlled by the frequency RANGE MHz selector and the band logic circuitry. The $f_c$ pulse output from the pre-scaler is applied to the counter/storage circuitry.

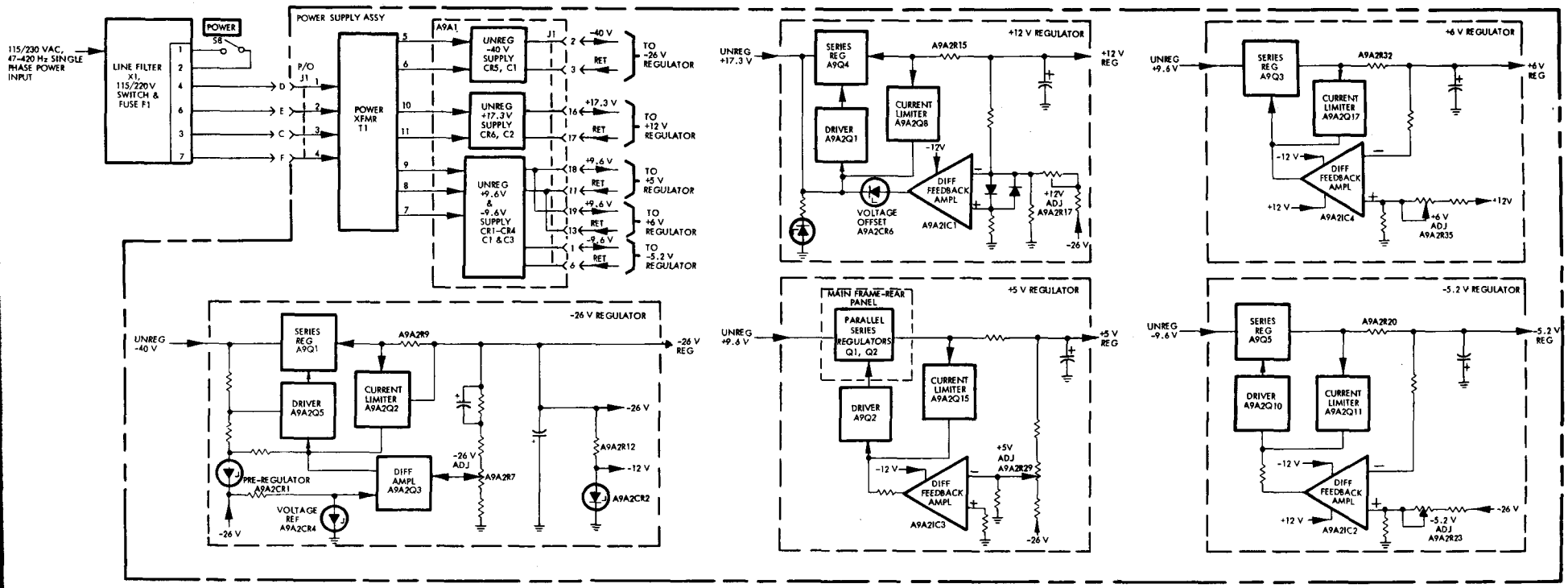
3-60. In the normal count mode, the duration of the count is controlled by the UPGATE command from the time base generator circuitry. The counter/storage circuitry counts the $f_c$ pulses for the duration of the UPGATE command ($\Delta T$) period, and then stores that number upon command from the time base generator circuitry. The storage has six four-bit BCD display outputs that drive the display. The count being stored is displayed by the six digit display assembly. After the count is stored, the time base generator circuitry clears the counter in preparation for the next cycle. Figure 3-9 shows the normal count mode timing sequence.

3-62. The time base generator circuitry controls the timing functions of the frequency counter and the frequency lock circuitry. Timing is derived from either a 4 MHz oscillator whose output is divided by four to obtain a stable 1 MHz signal; or an external stable 1 MHz signal. The selected




3-7

Figure 3-7. Band Center Command Circuitry, Detailed Block Diagram




3-18

*Figure 3-18. Regulated Power Supplies, Detailed Block Diagram*

# SECTION IV
# MAINTENANCE

## 4-1. GENERAL.

4-2. This section contains maintenance instructions for the Signal Generator. Included are a list of test equipment required to maintain the instrument, symptomatic and systematic troubleshooting procedures to localize a malfunction to an individual subassembly or circuit, detailed circuit theory, and calibration instructions for restoring the Signal Generator to proper operating condition after the necessary repairs and/or replacements have been effected.

## 4-3. TEST EQUIPMENT REQUIRED.

4-4. The test equipment required for the maintenance of the Signal Generator is listed in Table 4-1. Instruments of equivalent characteristics may be substituted for any item listed.

TABLE 4-1. TEST EQUIPMENT REQUIRED FOR MAINTENANCE

| | |
|---|---|
| 1. | Digital Voltmeter (AC/DC), Ballantine Model 355 |
| 2. | Frequency Counter, Eldorado Electrodata Model 1650 |
| 3. | Frequency Counter and Converter, Hewlett-Packard Model 5245L/5253B |
| 4. | Signal Generator, Hewlett-Packard Model 612A |
| 5. | Power Meter, General Microwave Model 454A |
| 6. | Thermistor Mount, General Microwave Model 421C |
| 7. | 80 MHz Scope, Tektronix Model 585 |
| 8. | Spectrum Analyzer, SINGER Model SA-70 |
| 9. | Oscilloscope, Hewlett-Packard Model 130C |
| 10. | Sweep Generator (10 to 550 MHz) Telonic Model 2003 |
| 11. | Standing Wave Indicator, Hewlett-Packard Model 415B |
| 12. | RHO-Tector, Telonic Model TRB-3 |
| 13. | Standard Mismatch Termination, Telonic Models TRMI-1.20 and TRMI-1.50 |
| 14. | 50-Ohm Termination, Telonic Type N |
| 15. | Step Attenuator, Kay Model 460A |
| 16. | Pad, 10 dB |
| 17. | Pad (Calibrated), 20 dB |
| 18. | BNC "T", UG-274/U |
| 19. | Type N to BNC Adapter, UG-201A/U |
| 20. | Detector, Hewlett-Packard Model 423A |
| 21. | Pad (Standard), 80 dB |
| 22. | Signal Generator, SINGER Model 6201 |
| 23. | Step Attenuator (Standard), 0-70 dB |
| 24. | Test Oscillator, Hewlett-Packard Model 651B |
| 25. | DC Digital Voltmeter, Hewlett-Packard Model 3450A |
| 26. | AC Digital Voltmeter, Fluke 8300A-01 |
| 27. | Dual Trace Plug-In, Hewlett-Packard Model 1405A |
| 28. | Pad, 6 dB |
| 29. | Matching Transformer, Applied Research Model 50-93 |
| 30. | 50-Ohm Series Resistor (1/4 watt metal film resistor mounted in coaxial package containing one male BNC connector and one femal BNC connector) |
| 31. | Subminiature-to-BNC Adapter, Sealectro Model 50-174-6800 |
| 32. | Subminiature Plug, Sealectro Model 51-007-0000 |
| 33. | Subminiature Jack, Sealectro Model 51-008-0000 |

## 4-5. TROUBLESHOOTING.

4-6. COMPONENT LOCATIONS.

4-7. The locations of the major assemblies and test points are illustrated in Figure 4-1. To gain access to these components, remove the top cover plate as directed in the following steps.

a. With the Signal Generator withdrawn from line power, loosen and remove the single screw (located at the center of the rear panel top lip) that secures the position of the top cover plate.

b. Grasp the cover plate and slide it to the rear of the Signal Generator until it is completely disengaged.

4 8 POWER SUPPLY CHECKS.

4-9. Improper operation of the Signal Generator may be due to a malfunction within power supply assembly A9 or one or more of the regulators within this circuitry delivering out-of-limit voltages. To ascertain that the individual power supplies are operating properly, or to localize a malfunction, proceed as directed in Table 4-2.

**NOTE**

The -26 volt supply serves as the reference for the +12, +5 and -5.2 volt supplies; and the +12 volt supply serves as a reference for the +6 volt supply. In addition, the +12 and -26 volt supplies provide +V and -V supplies, respectively, to the IC difference amplifiers in the +12, +6, +5 and -5.2 volt supplies. Consequently, if the -26 volt supply must be adjusted to obtain the proper output level, it will be necessary to check the output levels of the +12, +6, +5 and -5.2 volt supplies. Similarly, if the +12 volt supply output is adjusted, it will be necessary to check the output levels of the +6, +5 and -5.2 volt supplies.

TABLE 4-2. POWER SUPPLY CHECKOUT PROCEDURE

| Step | Procedure | Normal Indication |
|---|---|---|
| 1 | Check the output of the -26 volt supply by connecting the "high" lead of a Ballantine 355 Digital Voltmeter (set to the -100 VDC range) to any one of the "-26V ORN" terminals of TB2; connect the "common" lead to any of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of an H-P 130C oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and the oscilloscope display. | Voltmeter indicates between -25.50 and -26.50 volts; ripple is 1 millivolt peak-to-peak or less. Adjust A9A2R7 (Figure 4-2) is required. |
| 2 | Check the output of the +12 volt supply by connecting the "high" lead of the Ballantine 355 Voltmeter (set to the +100 VDC range) to any one of the "+12V RED" terminals of TB2; connect the "common" lead to any one of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and the oscilloscope display. | Voltmeter indicates between +11.50 and +12.50 volts; ripple is 2 millivolts peak-to-peak or less. Adjust A9A2R17 (Figure 4-2) if required. |
| 3 | Check the output of the -5.2 volt supply connecting the "high" lead of the Ballantine 355 Voltmeter (set to the -10 VDC range) to any one of the "-5.2V GRN; terminals of TB2; connect the "common" lead to any of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and the oscilloscope display. | Voltmeter indicates between -5.15 and -5.25 volts; ripple is 2 millivolts peak-to-peak or less. Adjust A9A2R23 (Figure 4-2) if required. |
| 4 | Check the output of the +5 volt supply by connecting the "high" lead of the Ballantine 355 Voltmeter (set to the +10 VDC range) to any one of the "+5V YEL" terminals of TB2; connect the "common" lead to any one of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and oscilloscope display. | Voltmeter indicates between +4.95 and +5.05 volts; ripple is 2 millivolts peak-to-peak or less. Adjust A9A2R29 (Figure 4-2) if required. |
| 5 | Check the output of the +6 volt supply by connecting the lead of the Ballantine 355 Voltmeter (set to the +10 VDC range) to any one of the "+6V BLU" terminals of TB2; connect the "common" lead to any one of the "GRD BLK" terminals of TB2. Connect the vertical input terminals of the oscilloscope (AC-coupled) to the same terminals as the voltmeter. Note both the voltmeter indication and oscilloscope display. | Voltmeter indicates between +5.95 and +6.05 volts; ripple is 10 millivolts peak-to-peak or less. Adjust A9A2R35 (Figure 4-2) if required. |

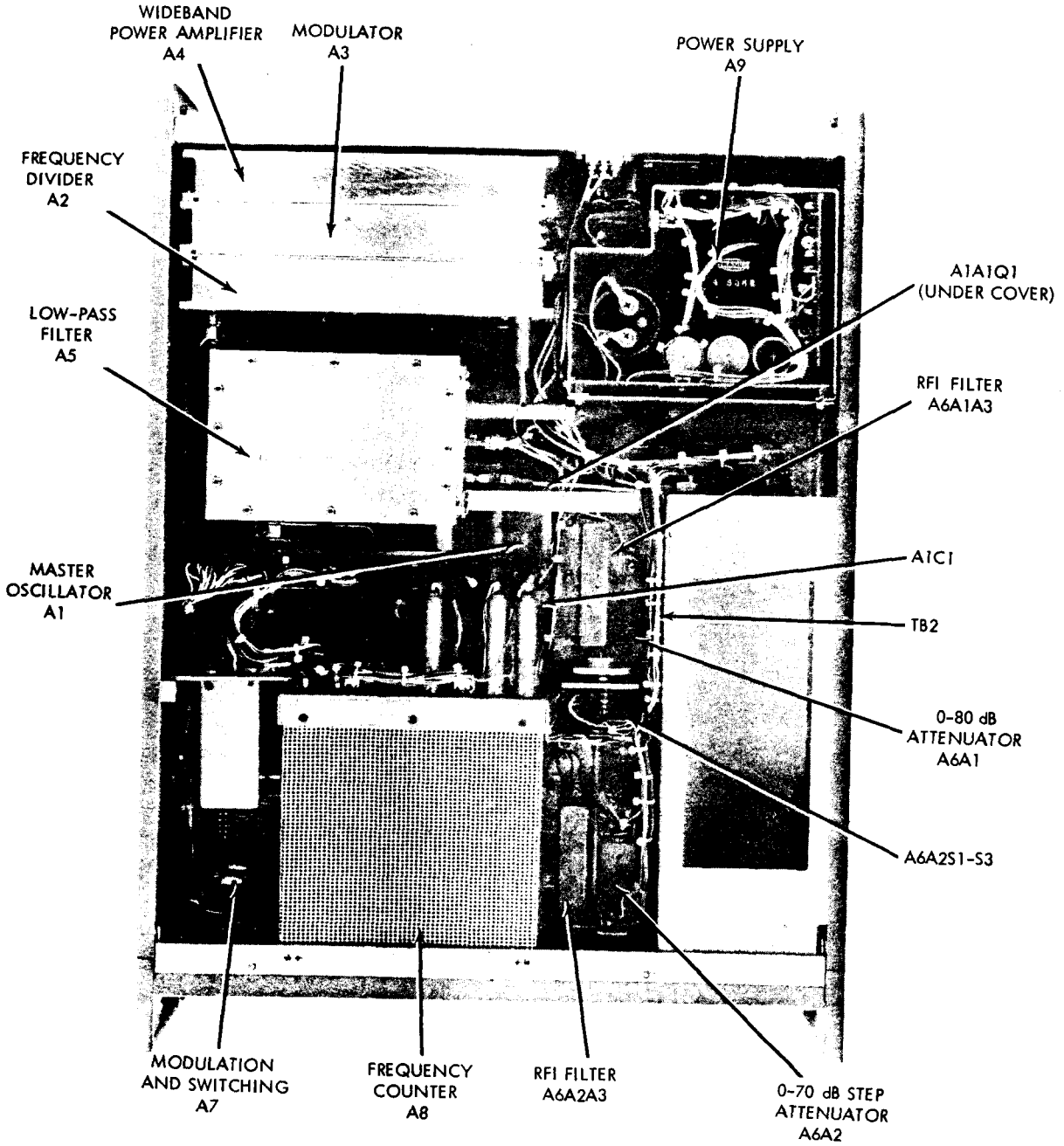



Figure 4-1. Top View of Signal Generator (Cover Removed)

4-10. TROUBLE LOCALIZATION.

4-11. The selectable frequency bands, modulation modes and frequency counter modes enable the technician to isolate a malfunction to a group of circuits by symptomatic troubleshooting procedures. Once the malfunction has been isolated to a particular circuit grouping, systematic trouble localization procedures will lead the technician to the defective component. Table 4-3 is a symptomatic troubleshooting guide which references the technician to the proper checkout, replacement and/or calibration procedure necessary to restore the Signal Generator to normal operating condition.

## 4-12. CHECKOUT PROCEDURES.

4-13. Paragraphs 4.14 through 4.47 detail the test procedures to be employed to determine whether an individual assembly within the Signal Generator is operating properly.

TABLE 4-3. SYMPTOMATIC TROUBLE LOCALIZATION GUIDE

| Symptom | Possible Cause and Checkout Procedure | Assembly No. | Paragraph |
|---|---|---|---|
| No RF output for any setting of the RANGE MHz and dBm switches; frequency counter functions only in external count operation. | 1. Master oscillator inoperative. | A1 | 4.14 |
| | 2. Frequency divider inoperative | A2 | 4.19 |
| | 3. Modulator inoperative. | A3 | 4.23 |
| No RF output for any setting of the RANGE MHz and dBm switches; frequency counter functions normally. | 1. Modulator inoperative. | A3 | 4.23 |
| | 2. Wideband power amplifier inoperative. | A4 | 4.26 |
| | 3. Low-pass filter inoperative. | A5 | 4.31 |
| | 4. Output attenuator inoperative. | A6 | 4.36 |
| | 5. Modulation and switching inoperative. | A7 | 4.40 |
| No RF output for one or more (but not all) settings of the RANGE MHz switch; frequency counter may or may not function normally. | 1. Frequency divider inoperative. | A2 | 4.19 |
| Excessive harmonic content in RF output; loss of RF power at upper half of any band. | 1. Oscillator board inoperative. | A8A3A6 | 4.42 |
| | 2. Low-pass filter inoperative. | A5 | 4.31 |
| No AM modulation | 1. Modulator inoperative. | A3 | 4.23 |
| | 2. Modulation and switching inoperative. | A7 | 4.40 |
| Excessive FM on AM | 1. Master oscillator defective. | A1 | 4.14 |
| | 2. Power supply defective. | A9 | 4.8 |
| 1 kHz internal modulation inoperative | 1. Modulation and switching inoperative. | A7 | 4.40 |
| No FM modulation | 1. Modulation and switching inoperative. | A7 | 4.40 |
| Frequency lock mode inoperative | 1. Low-pass filter inoperative. | A5 | 4.31 |
| | 2. AFC board inoperative. | A8A3A7 | 4.42 |
| No pulse modulation | 1. Modulator inoperative | A3 | 4.23 |
| | 2. Modulation and switching inoperative. | A7 | 4.40 |
| Frequency counter inoperative on one band only | 1. Low-pass filter inoperative | A5 | 4.31 |

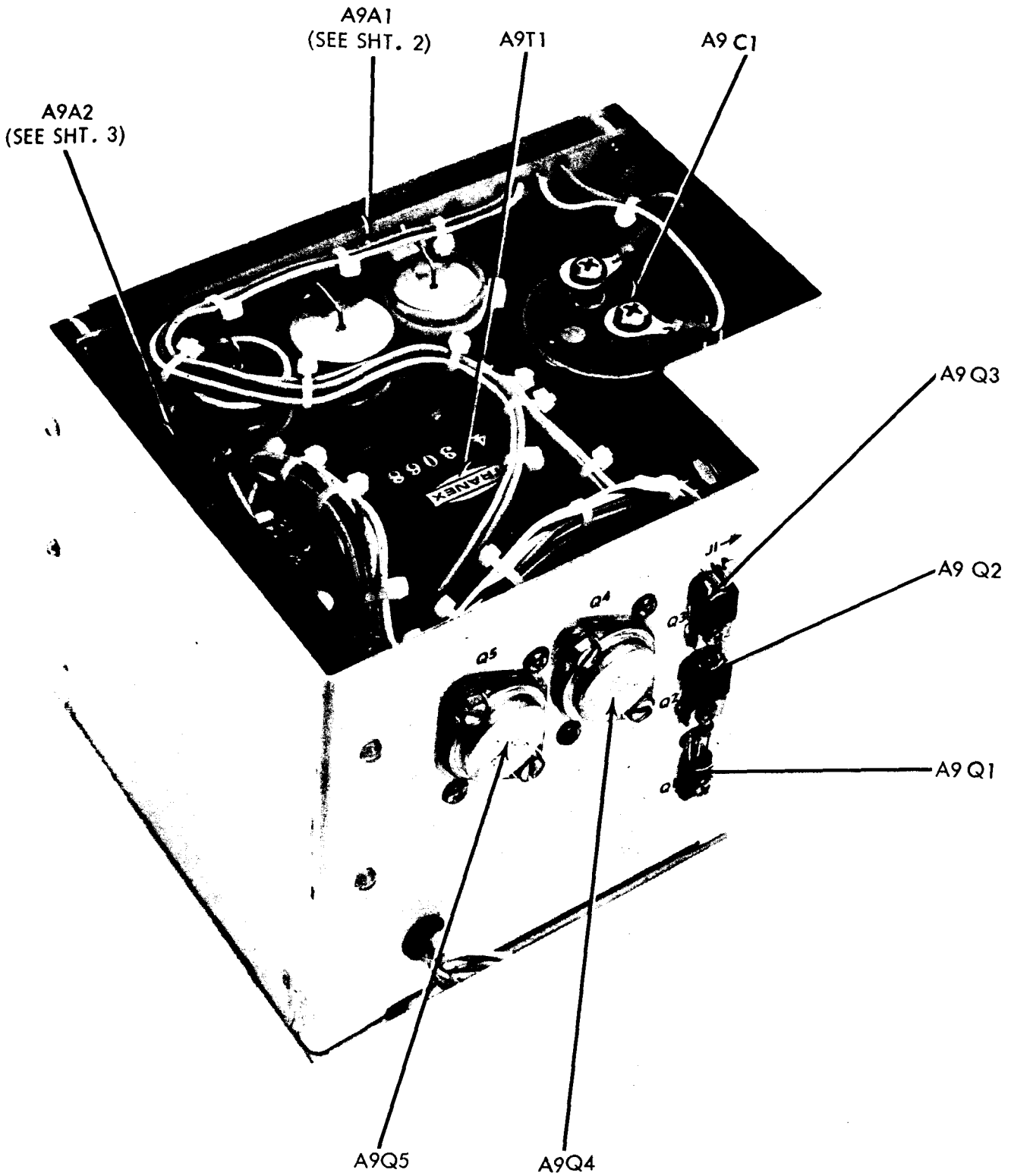



Figure 4-2. Power Supply **A9** (Sheet 1 of 3)

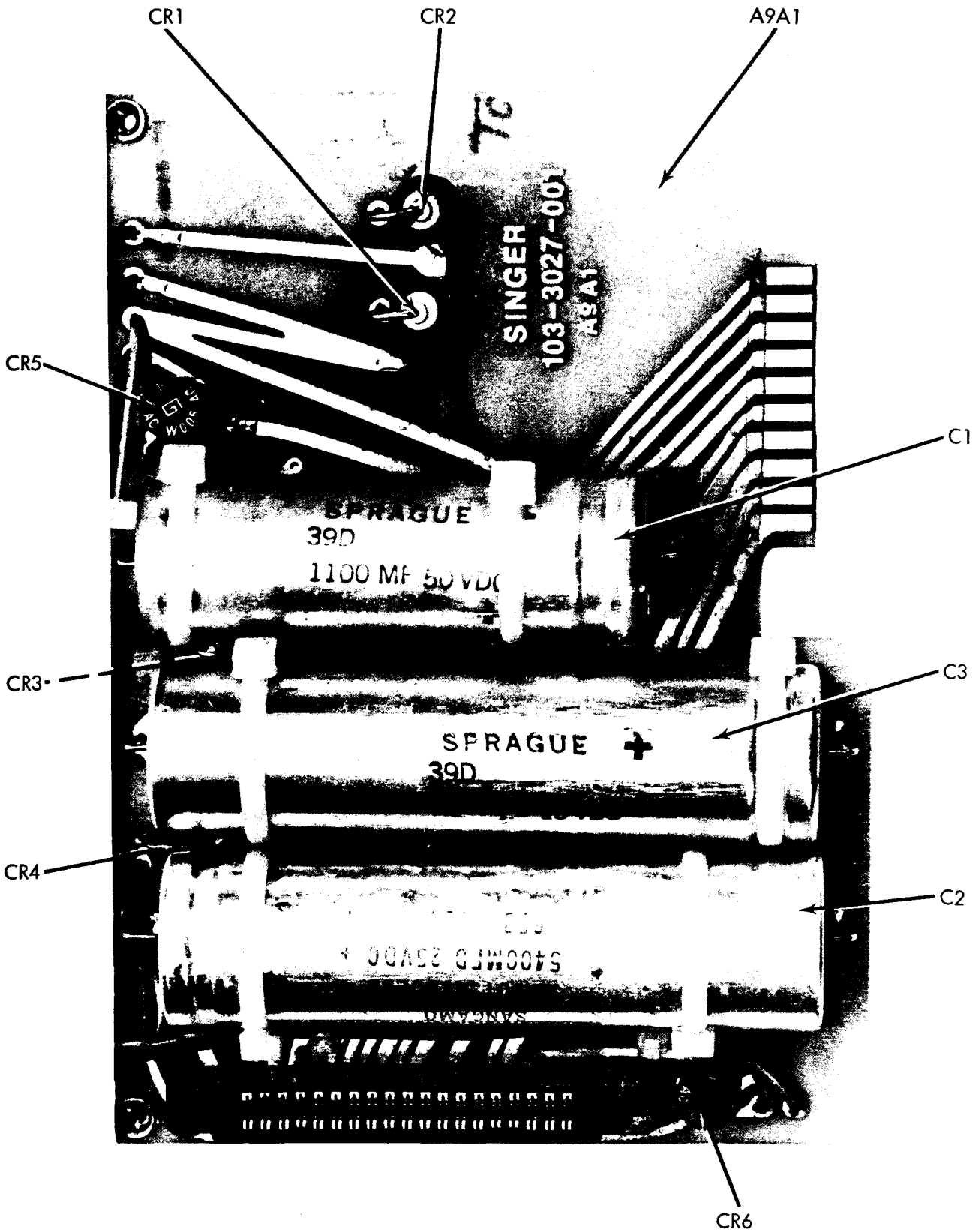



Figure 4-2. Power Supply **A9** (Sheet 2 of 3)

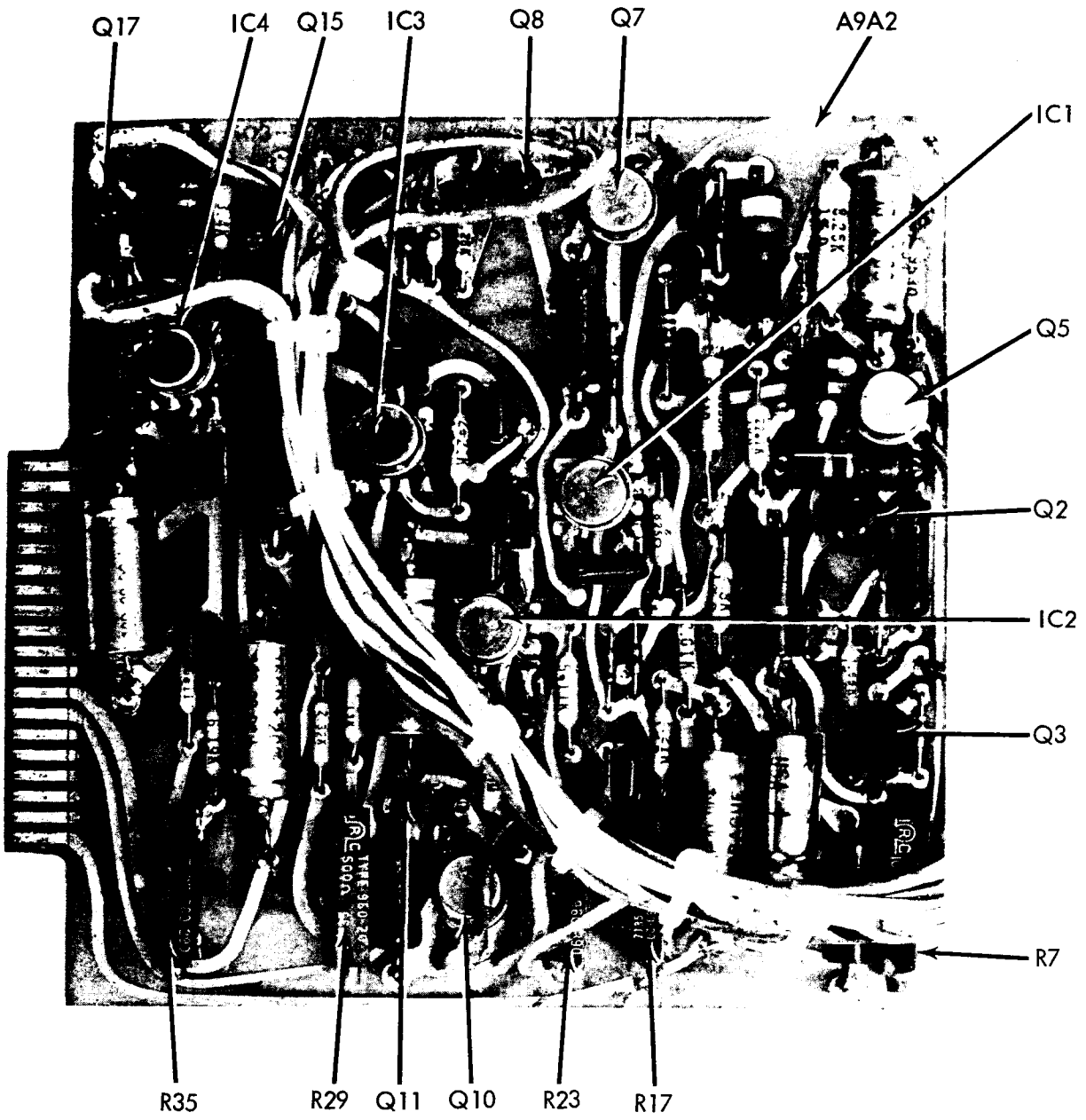



Figure 4-2. Power Supply **A9** (Sheet 3 of 3)

## 14 MASTER OSCILLATOR A1

4-15. Prior to performing the checks of paragraphs 4-16 through 4-18, check that the proper operating voltages are being applied to A1 (refer to Table 4-4).

4-16. Frequency Range.

a. Set the VERNIER frequency control to mid-range and with the CW pushbutton pressed, disconnect A2J1 from A1J1. Couple A1J1 to an H-P 5245L/5253B electronic counter/frequency converter through a 10 dB, 50 ohm pad.

b. Rotate the FREQUENCY control fully clockwise and determine the master oscillator output frequency; it should be at least 512 MHz. Rotate the FREQUENCY control fully counterclockwise and again determine the output frequency; it should be below 248 MHz. If both of these frequency indications are obtained, proceed to paragraph 4-17. Ohterwise, it may be necessary to reset the stop gear to be sure of a tuning range from 248 to 512 MHz.

**CAUTION**

Do not tune the oscillator above 525 MHz during the adjustment process; damage may result. (Typical OSC range from 520-246.)

4-17. Output Level.

a. With the VERNIER frequency control set to mid-range, the CW pushbutton is pressed, the FREQUENCY control rotated fully counterclockwise and A2P1 disconnected from A1J1, couple an H-P 478A/431C thermistor mount/power meter to A1J1 via a 10 dB, 50 ohm pad.

b. Note the power meter indication; it should read a minimum of -7 dBm (corresponding to a master oscillator output level of +3 dBm).

c. While continuously monitoring the power meter indication, slowly rotate the FREQUENCY control clockwise, until the high end stop is reached; the power meter should read at least -7 dBm throughout the band. If the output power requirements are obtained, proceed to paragraph 4-18.

4-18. Spurious Outputs.

a. Tune a Singer Model SA-70 Wide Dispersion Microwave Spectrum Analyzer to 500 MHz, a dispersion of 130 MHz/division, a bandwidth of 200 kHz, a sweep time of 3 msec/division and a logarithmic amplitude display. With no signal coupled to the analyzer, adjust the IF gain for a noise display one division high and set the RF attenuator for 30 dB insertion.

TABLE 4-4. ASSEMBLY POWER DISTRIBUTION

| Assembly | Voltage | Point of Application |
|---|---|---|
| Master Oscillator A1 | -26 volts<br>-26 volt return (ground) | A1C1 (violet lead of orange/black twisted pair from TB2).<br>Ground lug on A1C1 (black lead of orange/black twisted pair from TB2). |
| Frequency Divider A2 | +12 volts<br>-5.2 volts | A2FL1C2 (red lead of red/green twisted pair from A3).<br>A2FL1C1 (green lead of red/green twisted pair from A3). |
| Modulator A3 | +12 volts<br>-5.2 volts | A3A4C1 (red lead from TB2).<br>A3A4C2 (green lead from TB2). |
| Wideband Power Amplifier A4 | +12 volts<br>-5.2 volts | Junction of A4A1C67 and A4A1L37 (red lead from A3A5C1).<br>Junction of A4A1C69 and A4A1L40 (green lead from A3A5C2). |
| Low Pass Filter A5 | +6 volts<br>+5 volts<br>-26 volts<br>Ground | A5A1A5C1 (blue lead from TB2).<br>A5A3J1-19 & -W (yellow lead from TB2) via P1-19 & -W.<br>A5A3J1-3 (orange lead from TB2) via P1-3.<br>A5A3J1-1 & -A (black lead from TB2) via P1-1 & -A. |
| Output Attenuator A6 | +6 volts<br>Ground | A6A1A3C1 and A6A2A3C1 (blue lead from TB2).<br>Ground lug on A6 (black lead from TB2). |
| Modulation and Switching A7 | +12 volts<br>-26 volts<br>-5.2 volts<br>Ground | A7J1-V (red lead from TB2) via P2-V.<br>A7J1-12 (orange lead from TB2) via P2-12.<br>A7J1-U (green lead from TB2) via P2-U.<br>A7J1-D & -F (black lead from TB2) via P2-D & -F. |
| Frequency Counter A8 | +5 volts<br>-26 volts<br>Ground | A8P2-10 & -L (blue lead via A5A3J2-10 & -L.<br>A8P2-C (violet lead) via A5A3J2-C.<br>A8P2-1 & -A (black lead) via A5A3J2-1 & -A. |

b. With the VERNIER control set to mid-range, the CW pushbutton pressed and the FREQUENCY control set fully clockwise, couple A1J1 to the spectrum analyzer. Adjust the analyzer RF and/or IF attenuators to obtain a convenient display.

c. While continuously monitoring the spectrum analyzer display, slowly rotate the FREQUENCY control counterclockwise until the low frequency stop is reached. The master oscillator output should be continuous (i.e., no tearing or breaking-up).

## 4.19 FREQUENCY DIVIDER **A2**

4-20. To check assembly A2 for proper operation, first separate it from assembly A3 as directed in steps a through d of paragraph 4-147, temporarily replace assembly A2 into the Signal Generator as directed below and then perform the checks of paragraphs 4-21 and 4-22.

a. With the RANGE MHz switch set to 62-128, carefully place A2 into the Signal Generator so that the pin on the lever arm of A2A1S1 mates with the slot of the lever arm on the RANGE MHz switch shaft. Position A2 so that its two threaded mounting holes are directly above their mating holes on the main chassis bottom plate. Secure A2 to the bottom plate using two of the screws removed in step b of paragraph 4-147.

b. Check that the proper operating voltages are being applied to A2 (refer to Table 4-4).

4-21. Output Waveforms.

a. Set the RANGE switch to 248-512 and rotate the FREQUENCY control fully counterclockwise.

b. Couple A2P1 to A1J1. Insert the tip of an oscilloscope probe into the center conductor of A2J1; connect the probe ground lead to A2 ground. Couple the probe to the input of a Tektronix 561B sampling oscilloscope.

c. Observe the oscilloscope display; a waveform similar to that illustrated in Figure 4-3 should appear. Slowly rotate the FREQUENCY control throughout its tuning range, while monitoring the display; the display should be similar to Figure 4-3 at all frequencies within the band.

d. Repeat step c with the RANGE MHz switch set, in sequence, to 124-256, 62-128, 31-64, 15.5-32 and 7.75-16.

e. Disconnect W2P1 from A2J2 and couple the sampling scope to A2J2. Repeat step c.

f. Disconnect P6 from A2J3 and couple the sampling scope to A2J3. Repeat step c.

g. If the required output waveforms are obtained, proceed to paragraph 4-22; if they are not, remove the shield plate from A2 (refer to paragraph 4-147e) and effect the necessary repairs and/or replacements (refer to Table 4-12 and see Figure 4-4).

4-22. Output Power.

a. Couple A2J1 to an H-P 478A/431C thermistor mount/power meter through a 6 dB pad. Set the RANGE MHz switch to 248-512 and slowly rotate the FREQUENCY control throughout its range while noting the power meter reading; the power meter should indicate at least -36 dBm (corresponding to a minimum frequency divider output level of -30 dBm) throughout the band. Repeat the above for RANGE MHz switch settings of 124-356, 62-128, 31-64, 15.5-32 and 7.75-16.

b. Connect a Tektronix 585 oscilloscope to A2J2 and again rotate the FREQUENCY control throughout its range; the peak-to-peak indication should be at least 2.0 volts.

c. Connect the oscilloscope to A2J3 and again rotate the FREQUENCY control throught its range; the peak-to-peak indication should be at least 0.65 volt.

## 4.23 MODULATOR **A3**

4-24. To check assembly A3 for proper operation, first separate it from assembly A4 (refer to steps a and b of paragraph 4-148) and then replace both A2 and A3 back into the main chassis (refer to step a of paragraph 4-20). Check that the required operating voltages are being applied (refer to Table 4-4).

a. Set the front panel controls as indicated below.

| Control | Setting |
|---|---|
| RANGE MHz switch | 248 - 512 |
| FREQUENCY control | Mid-range |
| CW pushbutton | Pressed |
| dBm continuous control | Fully clockwise |
| VX2 pushbutton | Released |
| AM/FM switch | AM |

b. Connect A2P1 to A1J1 and couple A3A2P2 to an H-P 478A/431C thermistor mount/power meter. Note the power meter indication; it should read at least -18 dBm.

c. Set the RANGE MHz switch, in sequence, to 124-256, 62-128, 31-64, 15.5-32 and 7.75-16 and for each setting, note the power meter indication; it should be at least -25 dBm.

d. Disconnect the thermistor mount/power meter from A3A2P2. Tune a Singer Model SA-70 Wide Dispersion Microwave Spectrum Analyzer to 600 MHz, set for a dispersion of 300 Hz/division, a bandwidth of 200 kHz, a sweep speed of 3 msec/division and a logarithmic amplitude display. Set the RF input attenuator for 30 dB insertion and adjust the IF gain control to obtain a noise display one division high.

e. Couple the spectrum analyzer to A3A2P2 and adjust the FREQUENCY control to center the signal pip on the analyzer display. Adjust the analyzer RF and IF attenuators to obtain a full-scale display.

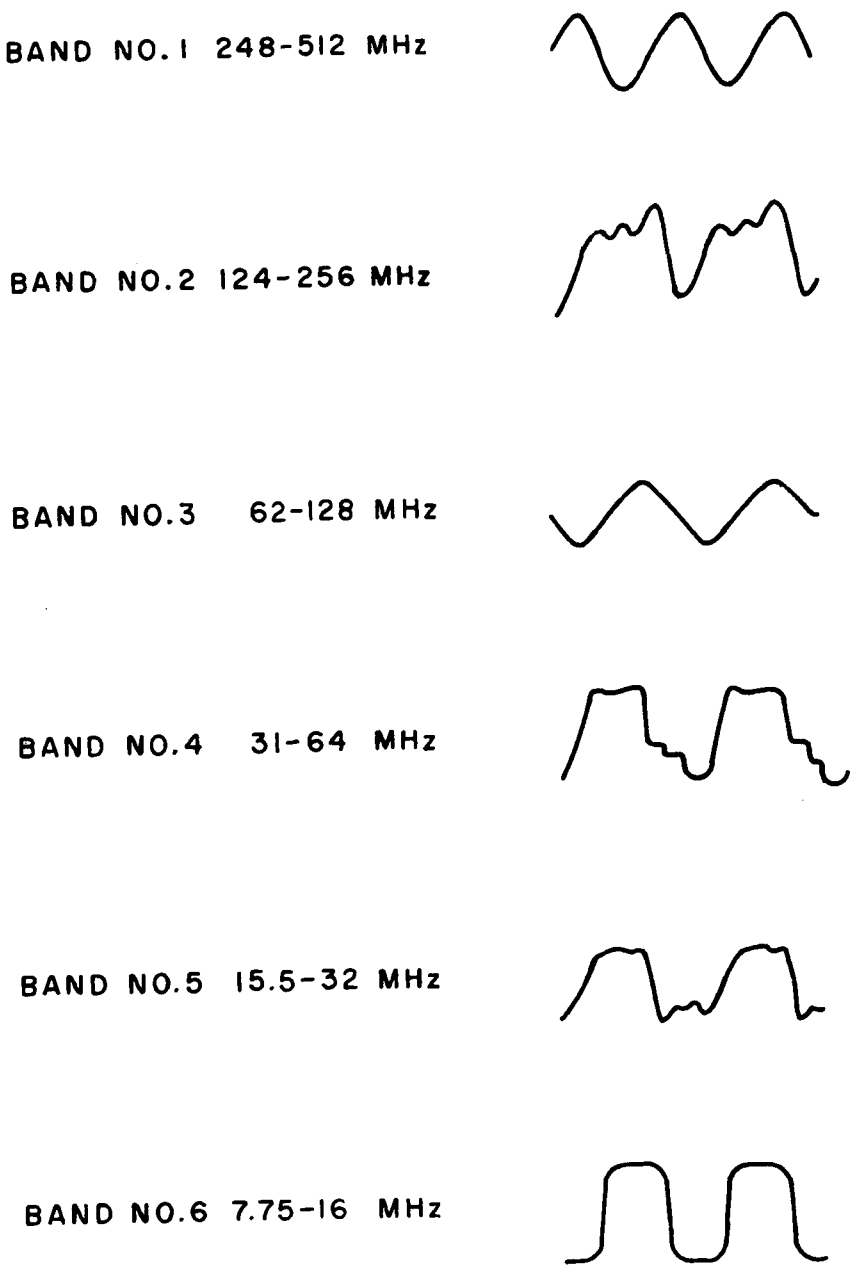



Figure 4-3. Typical Frequency Divider Output Waveforms

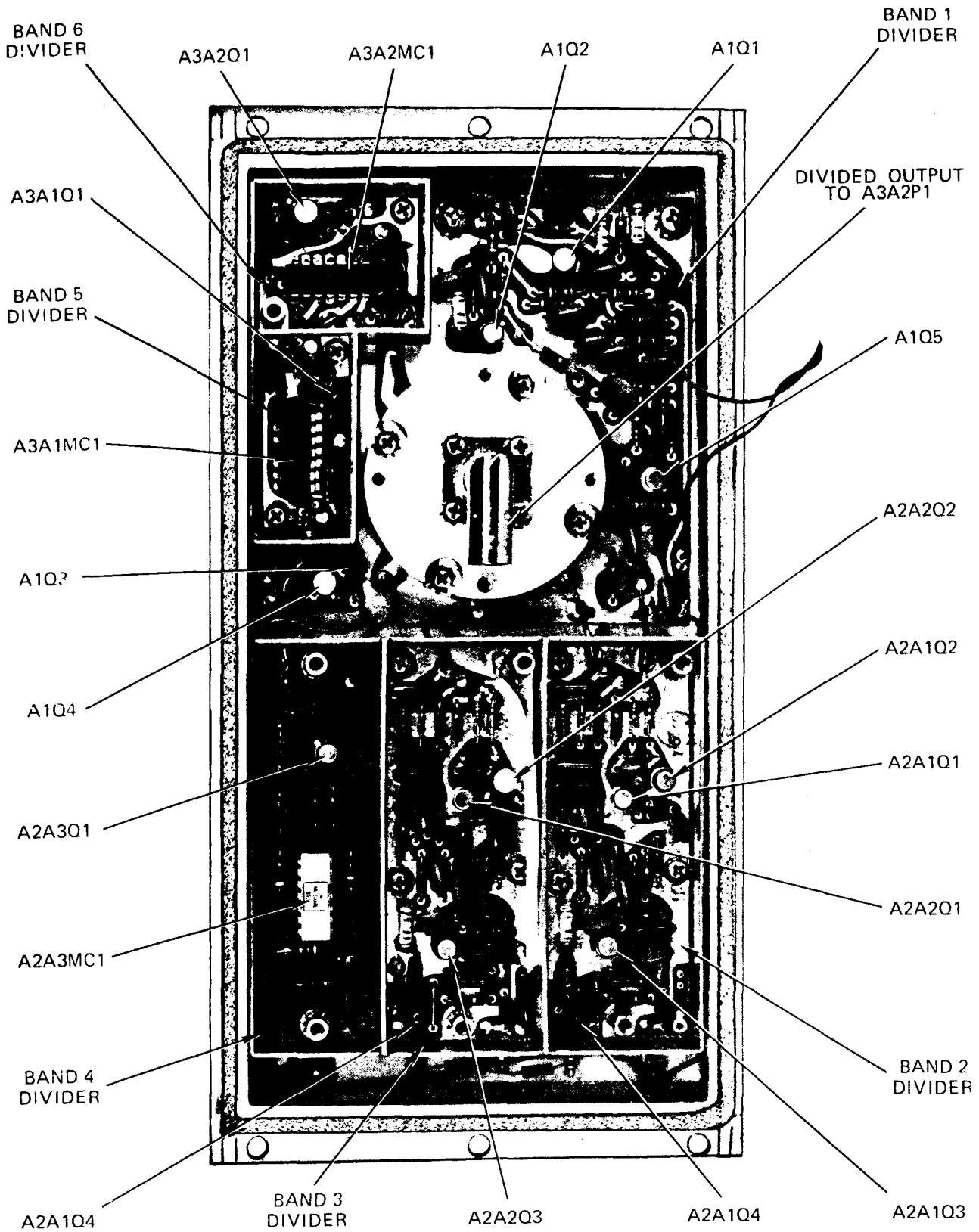



Figure 4-4. Frequency Divider Assembly **A2**

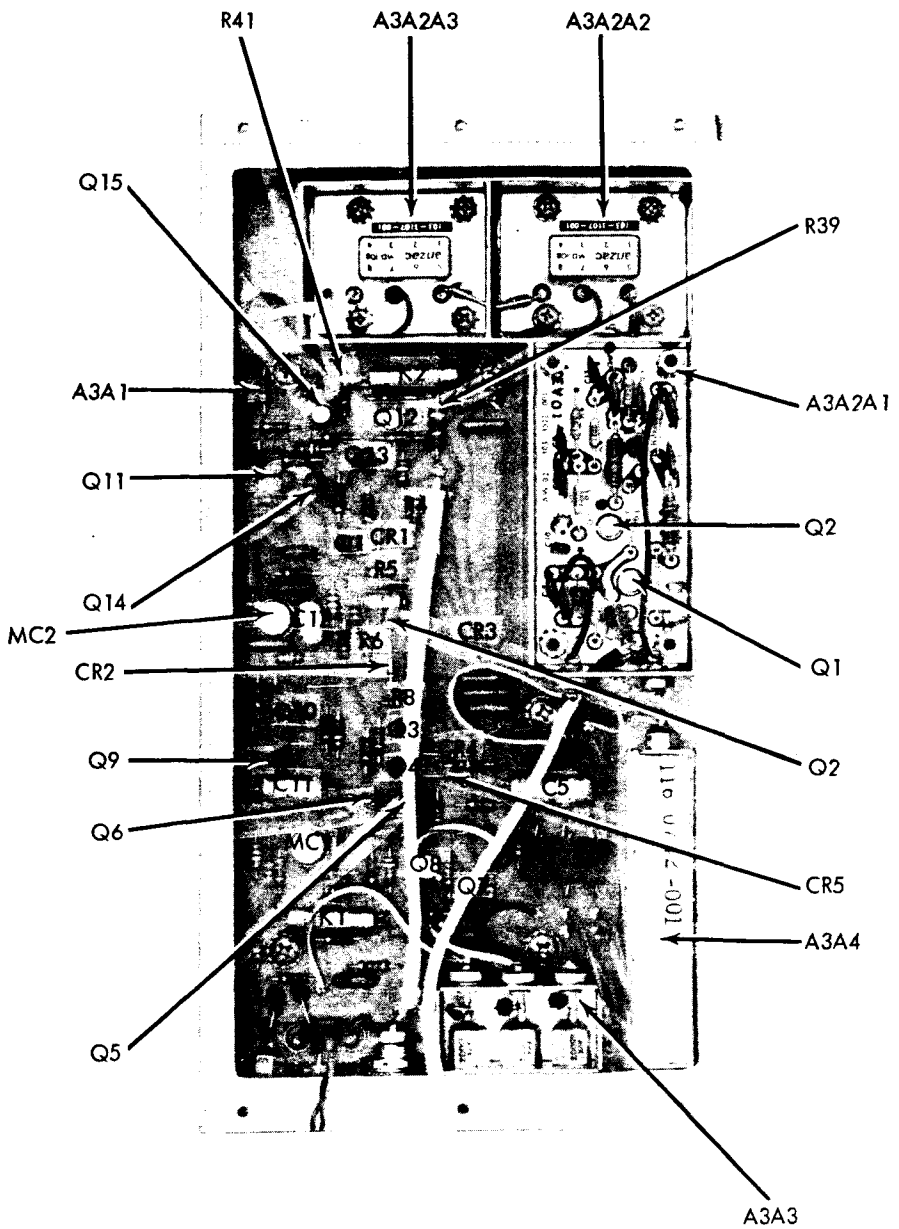



Figure 4-5. Modulator Assembly **A3**

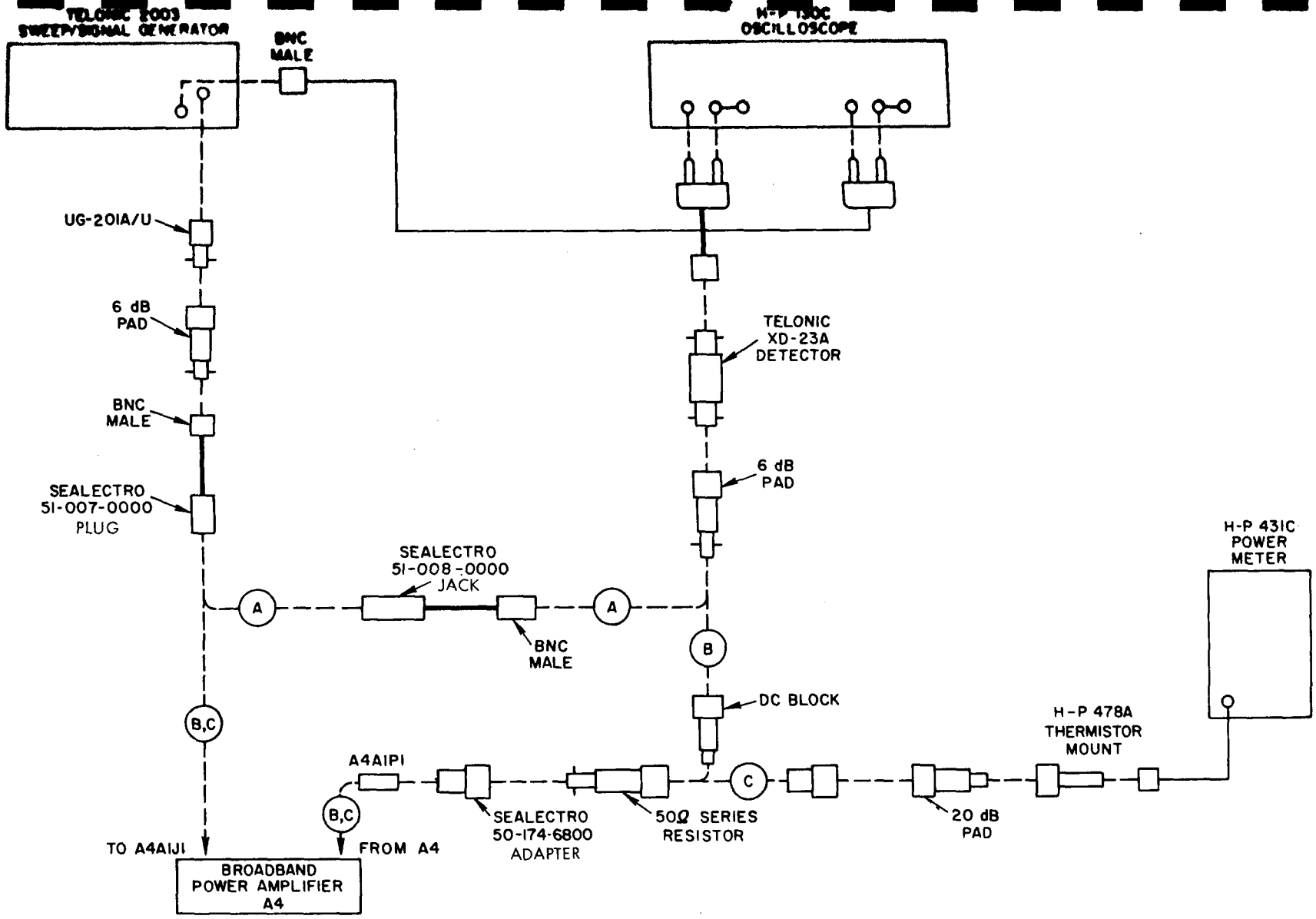



Figure 4-6. Equipment Setup for Wideband Power Amplifier Checkout

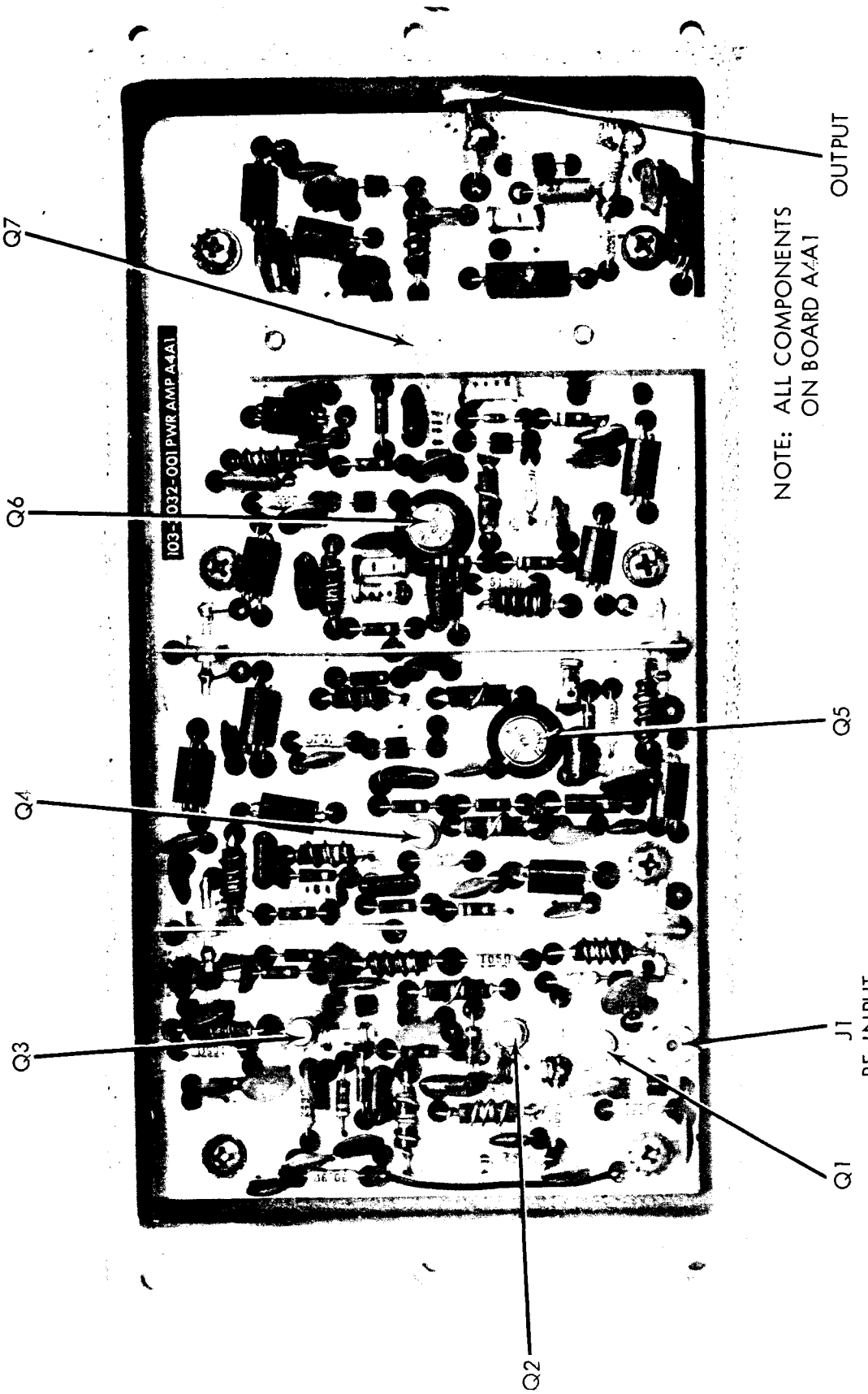



Figure 4-7. Wideband Power Amplifier **A4**

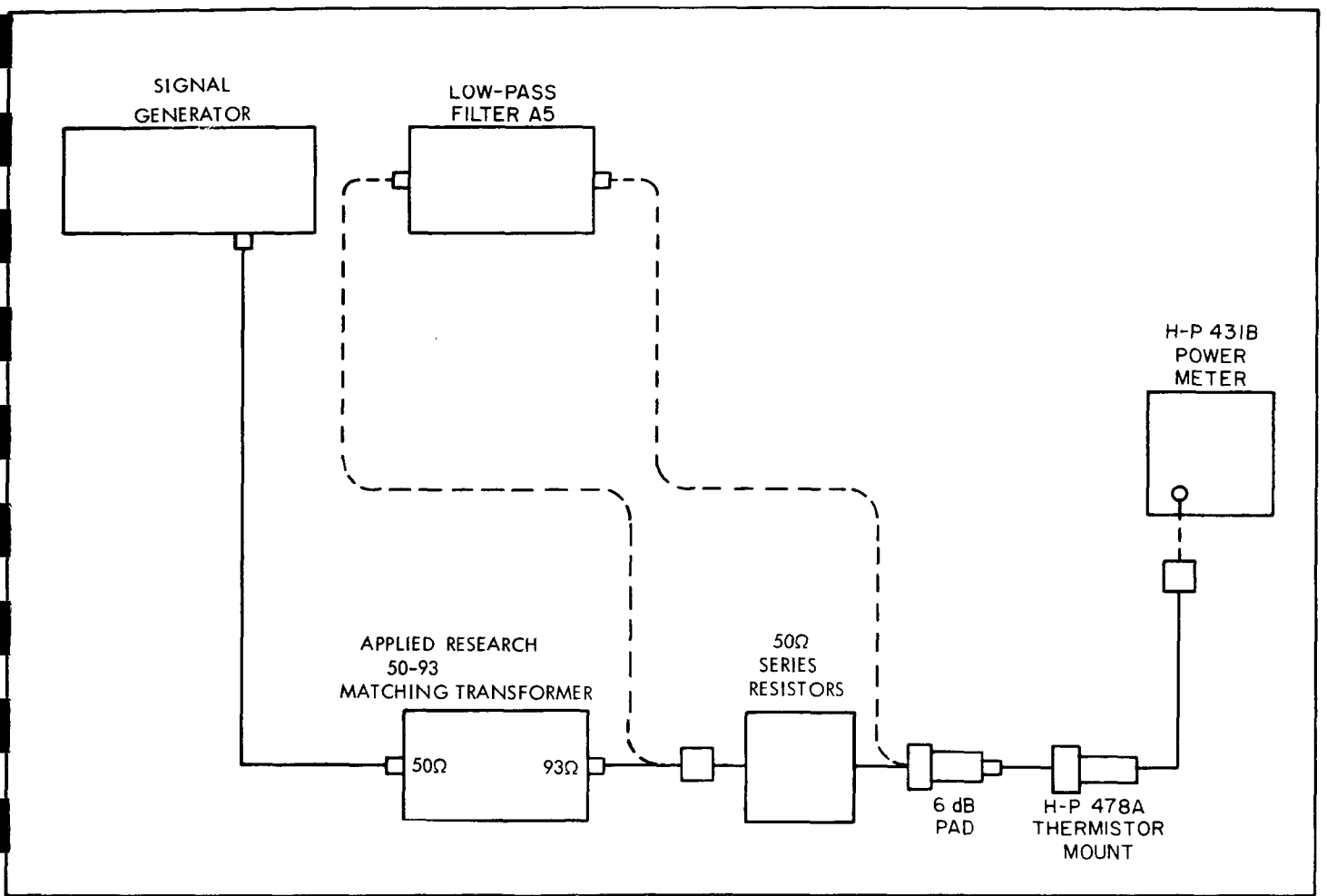



Figure 4-8. Equipment Setup for Low-Pass Filter Checkout

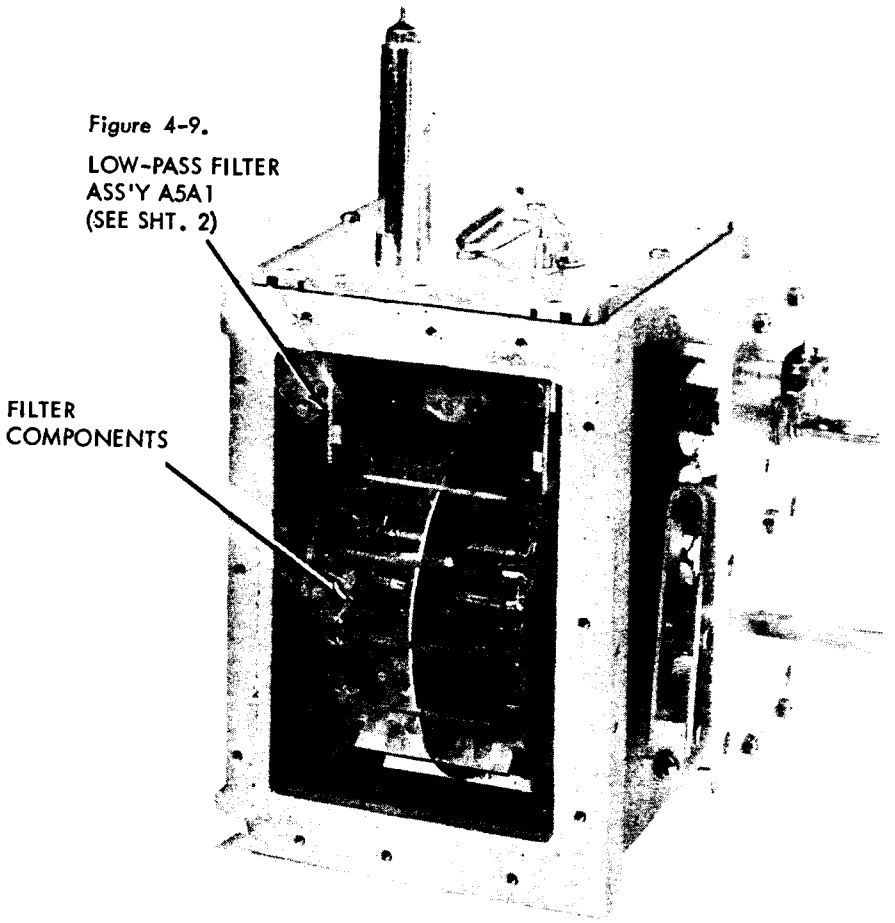



Figure 4-9. Low Pass Filter Assembly A5 (Sheet 1 of 2)

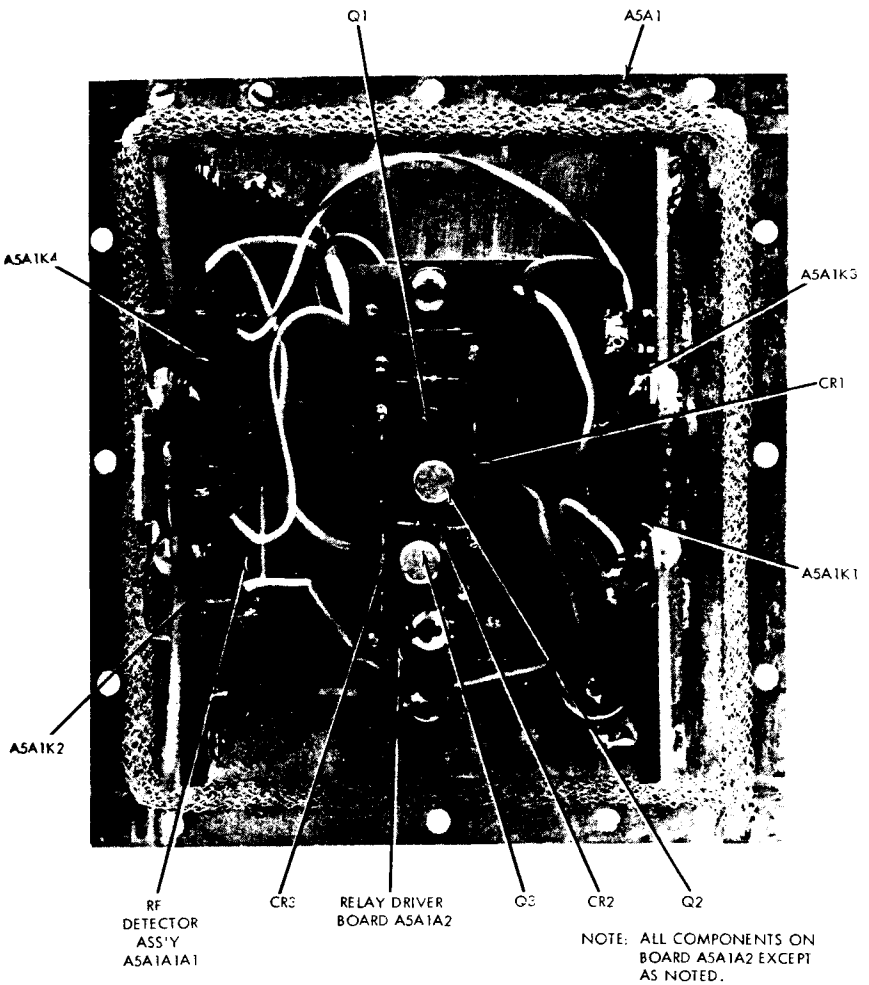



Figure 4-9. Low-Pass Filter Assembly **A5** (Sheet 2 of 2)

4-34. Band Logic Outputs. Place the EXT COUNT pushbutton in the released position. Using a Ballantine Model 355 Digital Voltmeter, ascertain that the proper output voltages are provided at the terminals of A5A3IC1 as a function of RANGE MHz switch and FM CAL pushbutton (refer to Table 4-6).

TABLE 4-6. BAND LOGIC OUTPUT LEVELS

| RANGE MHz Switch Setting | Test Point | | | |
|---|---|---|---|---|
| | A5A3IC1-3 | A5A3IC1-6 | A5A3IC1-8 | A5A3IC1-11 |
| 48-512 | 1 | 1 | 1 | 1 |
| 24-256 | 0* | 1 | 1 | 1 |
| 62-128 | 1 | 0* | 1 | 1 |
| 31-64 | 1 | 1 | 0* | 1 |
| 5.5-32 | 0* | 1 | 0* | 1 |
| .75-16 | 1 | 0* | 0* | 1 |

Notes: 1 ("high") level is +2.4 volts or greater
0 ("low") level is between 0 and +0.4 volts

* 1 level when FM CAL pushbutton is pressed

4-35. Frequency Lock Flip-Flop Outputs. Connect a Ballantine Model 355 Digital Voltmeter to terminal 8 of A5A3IC2 (LOCK command output). With the EXT COUNT pushbutton in the released position, momentarily set the NORMAL/LOCK switch to the NORMAL position. A level of between 0 and +0.4 volts DC should be observed on the digital voltmeter and the LOCK indicator should not be lit. Then, momentarily set the NORMAL/LOCK switch to the LOCK position. A level of +2.4 volts DC (or greater) should be observed on the digital voltmeter and the LOCK indicator should be lit. Change the position of the RANGE MHz selector switch or press the EXT COUNT on FM CAL pushbutton and observe that the LOCK indicator goes out.

## 4-36 OUTPUT ATTENUATOR **A6**

4-37. The output attenuator assembly consists of two sections; a 0 to 80 dB step attenuator (A6A1) and a 0 to 70 dB step attenuator (A6A2). Prior to checking these assemblies, ascertain that the proper operating voltages are being applied (refer to Table 4-4).

4-38. 0 to 80 dB Step Attenuator A6A1.

a. Perform steps a through d of paragraph 4-153 and slide A6A1 toward the rear of the main frame.

b. Using a voltmeter set to the 10 VDC range, measure voltage at the 80 dB eyelet on lamp board A6A1A1 for each position of the attenuator dBm switch. There should be +6 VDC present at the switch positions as indicated in Table 4-7. Check the contacts of switch A6A2S3 and/or lamp A6A1A1DS1 if specified voltages are not obtained.

TABLE 4-7. STEP ATTENUATOR CONTROL VOLTAGES

| dBm Switch Setting | A6A1A1 Test Point | A6A2A2 Test Point | | |
|---|---|---|---|---|
| | "80 dB" Eyelet | "10 dB" Eyelet | "20 dB" Eyelet | "40 dB" Eyelet |
| -10/1.0 V | +6 V | +6 V | +6 V | +6 V |
| 0/0.3 V | +6 V | 0 V | +6 V | +6 V |
| -10/.10 V | +6 V | +6 V | 0 V | +6 V |
| -20/.03 V | +6 V | 0 V | 0 V | +6 V |
| -30/10 mV | +6 V | +6 V | +6 V | 0 V |
| -40/3 mV | +6 V | 0 V | +6 V | 0 V |
| -50/1.0 mV | +6 V | +6 V | 0 V | 0 V |
| -60/0.3 mV | +6 V | 0 V | 0 V | 0 V |
| -70/.10 mV | 0 V | +6 V | +6 V | +6 V |
| -80/.03 mV | 0 V | 0 V | +6 V | +6 V |
| -90/10 µV | 0 V | +6 V | 0 V | +6 V |
| -100/3 µV | 0 V | 0 V | 0 V | +6 V |
| -120/0.3 µV | 0 V | 0 V | +6 V | 0 V |
| -130/.10 µV | 0 V | +6 V | 0 V | 0 V |
| -140/.03 µV | 0 V | 0 V | 0 V | 0 V |

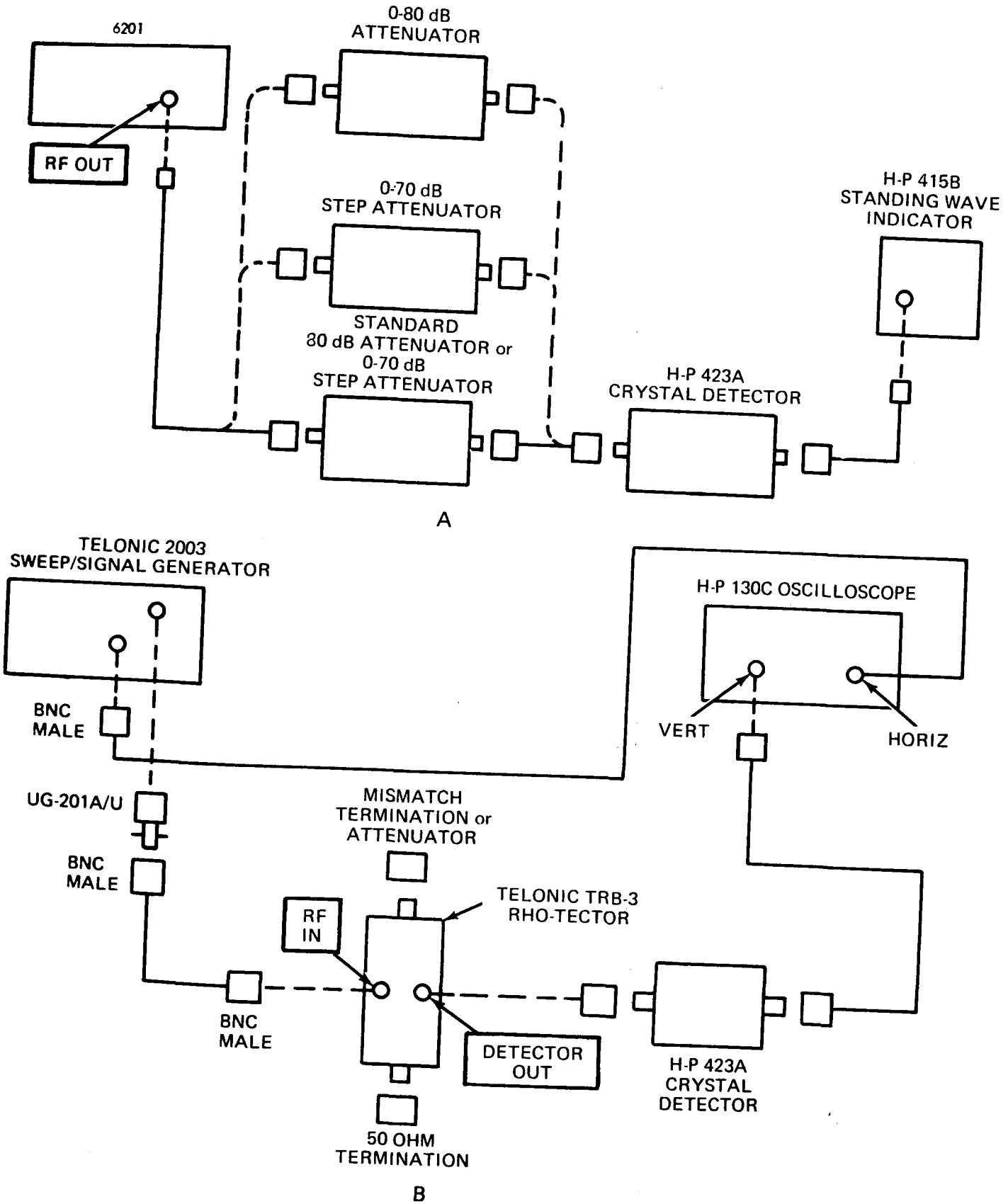



Figure 4-10. Equipment Setup for 0-80 dB and 0-70 dB Step Attenuator Checkout

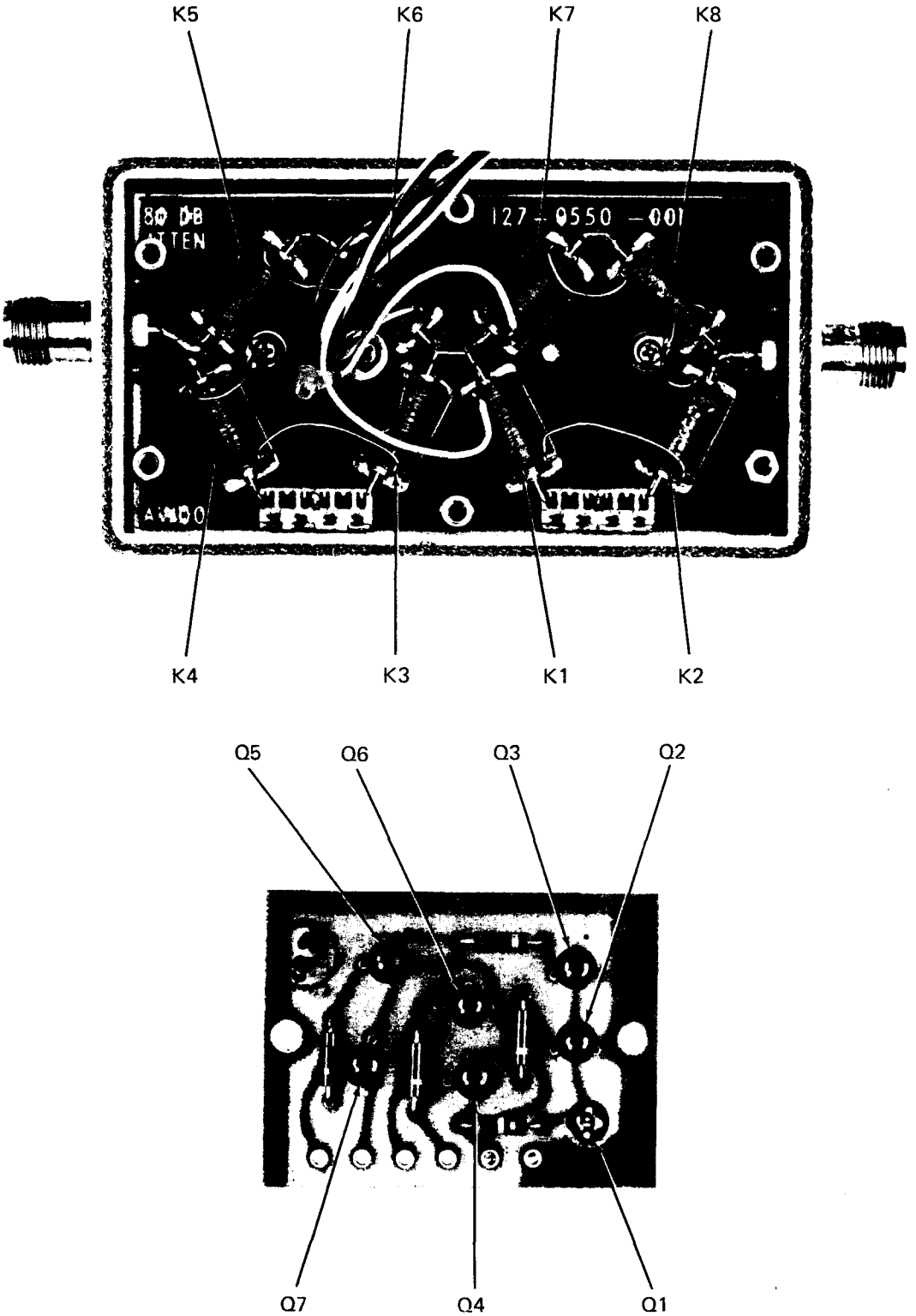
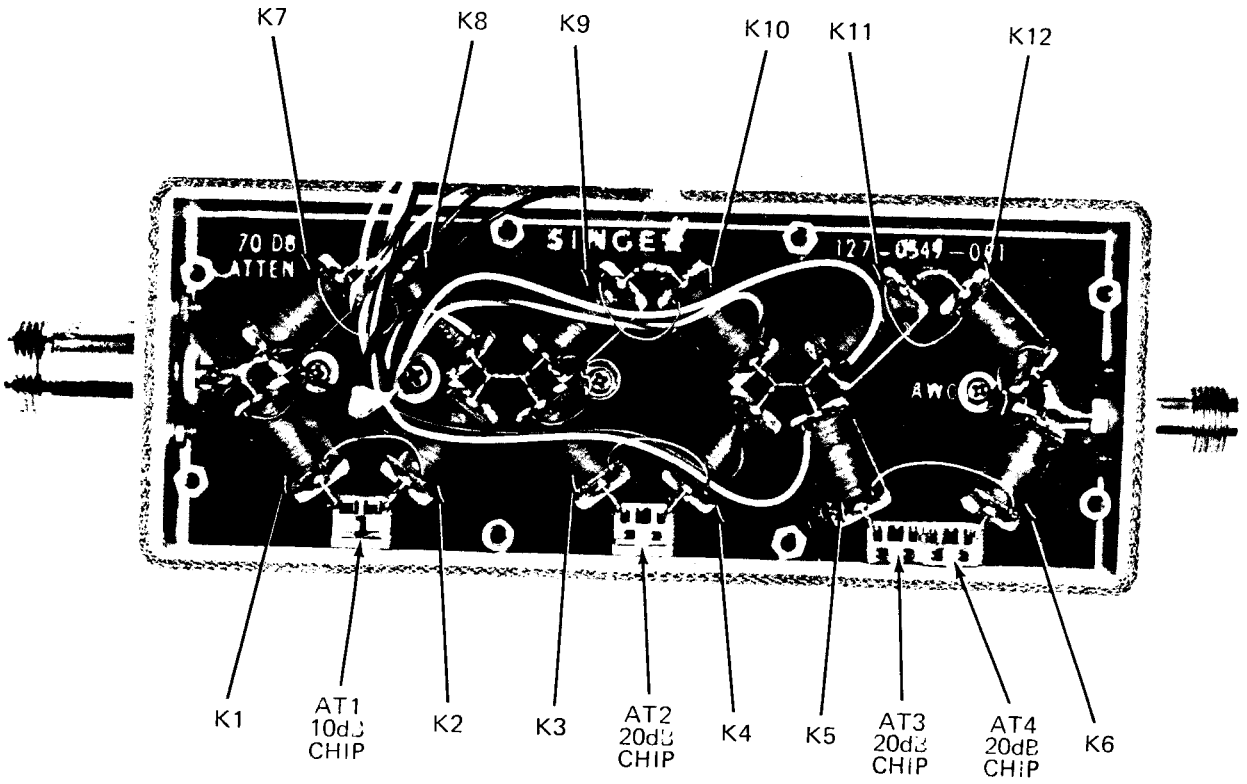



Figure 4-11. 0-80 dB Attenuator A6A1



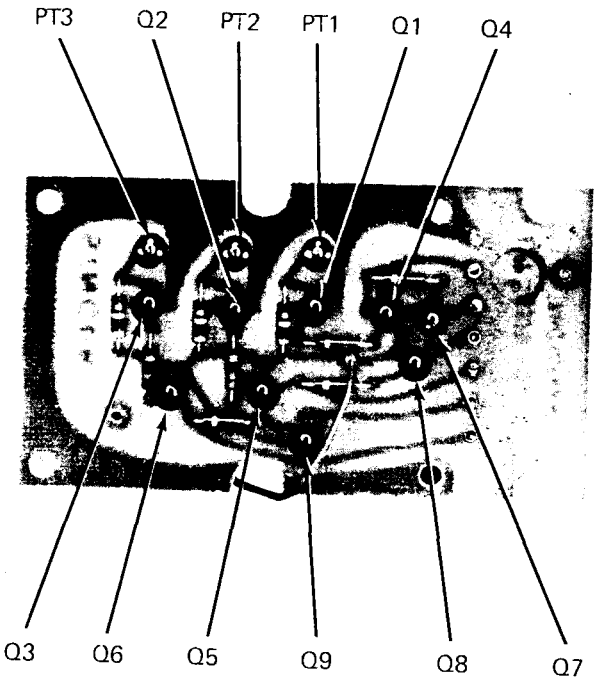




Figure 4-12. 0-70 dB Step Attenuator A6A2

c. Set the attenuator dBm switch to +10/1.0V.

d. Interconnect a standard 80 dB attenuator in the test setup of Figure 4-10A and set the attenuation to 0 dB. Tune the 6201 for a -40 dB output at 10 MHz and 50% AM. Adjust the 6201 modulating frequency to peak the response of the standing wave ratio indicator.

e. Adjust the standing wave indicator to obtain a reference reading of 1 dB on the SWR indicator normal meter scale.

f. Set the dBm switch to +10/1.0V position and connect the 80 dB attenuator under test in the test configuration of Figure 4-10. Note the reading (insertion loss) on the SWR indicator. It should not differ by more than 0.1 dB from the reference.

g. Repeat steps d, e, and f with the 6201 tuned to 500 MHz. Insertion loss should be 0.3 dB maximum at 500 MHz.

h. Set the standard attenuator to its 80 dB position and the dBm switch to -70/.10 mV.

i. Increase the 6201 output to +20 dBm and set the SWR indicator to the 50 dB range.

j. Adjust the SWR indicator for a -1 dB reference reading on the normal scale.

k. Connect the 80 dB attenuator under test in place of the standard attenuator and note the SWR indicator reading. It should be 80 dB ±0.7 dB.

l. Repeat steps i, j, and k with the 6201 tuned to 10 MHz. Attenuation should be 80 dB ±0.7 dB.

m. Malfunctions of this assembly can be located by reference to the assembly schematic diagram in conjunction with the voltage data furnished in Table 4-16. Component locations are shown in Figure 4-11.

4-39. 0-70 dB Step Attenuator.

a. Perform steps a, b, d and e of paragraph 4-152. Slide A6A1 towards the rear of the main frame.

b. Using a voltmeter set to the +10 VDC range, measure voltage at the 10 dB, 20 dB, and 40 dB eyelets on lamp board A6A2A2. There should be +6 VDC present at the dBm switch positions as indicated in Table 4-7. Check the contacts of switches A6A2S1 and A6A2S2 and/or lamp A6A2A2DS1, DS2 or DS3 if specified voltages are not obtained.

c. Interconnect a Telonic 2003 sweep generator, Telonic TRB-3 Rho-tector, H-P 423A detector and H-P 130C oscilloscope as shown in Figure 4-108. Affix the standard 1.25:1 mismatch termination and 50 ohm termination on the Rho-tector as shown in the figure.

d. Adjust the sweep generator and oscilloscope for a full-scale swept VSWR display. Note the 1.25:1 VSWR point.

e. Connect the output connector on the 0-70 dB step attenuator in place of the mismatch termination and terminate the input connector with 50 ohms.

f. Set the attenuator dBm switch to the +10/1.0V (0 dB), 0/0.3V (10 dB), -10/.10V (20 dB) and -30/10 mV (40 dB) positions and note the VSWR indication on the oscilloscope. It should be 1.25:1 maximum for all positions.

g. Repeat steps f and g with the 0-70 dB attenuator input connected in place of the mismatch termination. Terminate the output connector with 50 ohms. VSWR should be 1.25:1 maximum for all positions.

h. Perform step d of paragraph 4-38, except substitute a standard 0-70 dB step attenuator.

i. Adjust the standing wave ratio indicator gain to obtain a reference reading of -0.5 dB on the expanded meter scale.

j. Set the step attenuator under test for 0 dB (dBm switch at +10/1.0V) and connect it in place of the standard 0-70 dB attenuator. Note the reading (insertion loss) on the SWR indicator. It should not differ by more than 0.1 dB.

k. Repeat step j, setting the attenuator dBm switch, SWR indicator range and/or 6201 output level as indicated in Table 4-8 and note the SWR reading.

**NOTE**

Adjust the 6201 output and/or the SWR indicator range as necessary to maintain the 0.5 dB reference reading.

l. Set the 6201 to 500 MHz and repeat steps i through k. The same accuracy should be obtained.

m. Malfunctions of this assembly can be located by reference to the assembly schematic diagram in conjunction with the voltage data furnished in Table 4-16. Component locations are shown in Figure 4-12.

TABLE 4-8. 0-70 dB STEP ATTENUATOR CHECKOUT

| dBm Switch Setting | SWR Indicator "Range" Switch Setting | 6201 Signal Generator Output Level | SWR Indicator Reading (max)* |
|---|---|---|---|
| 1/0.3 V | 40 | -40 dBm | 1 ±0.15 dB |
| -10/.10 V | 20 | -20 dBm | 1 ±0.30 dB |
| -20/.03 V | 30 | -20 dBm | 1 ±0.45 dB |
| -30/10 mV | 40 | -20 dBm | 1 ±0.60 dB |
| -40/3 mV | 20 | 0 dBm | 1 ±0.75 dB |
| -50/1.0 mV | 30 | 0 dBm | 1 ±0.90 dB |
| -60/0.3 mV | 40 | 0 dBm | 1 ±1.05 dB |

* Maximum cumulative error should not exceed ±1.05 dB.

## 4-40 MODULATION AND SWITCHING ASSEMBLY **A7**.

4-41. A malfunction within this assembly can be located using signal tracing techniques in conjunction with the information provided in Table 4-7. To gain access to assembly A7, perform steps a and e of paragraph 4-155 and then carefully slide the counter assembly back and turn it over so that the assembly rests on low-pass filter assembly A5. The locations of the components on A7 are shown in Figure 4-13.

## 4-42 FREQUENCY COUNTER **A8**

4-43. To check assembly A8 for proper operation, first remove the assembly as described in paragraph 4-155, disassemble it as described below and then perform the checks of paragraphs 4-44 and 4-45. Refer to paragraph 4-46 for limited troubleshooting of the counter. The locations of components on A8 are shown in Figure 4-14.

a. Remove the three screws on the top and the six screws on the bottom of the assembly, and gently remove the case from A8.

b. Remove the three screws which fasten the printed circuit board retainer plate to the assembly.

**CAUTION**

To prevent possible damage to assembly A8, mount it on a sheet of paper or plastic before performing step c.

c. Reconnect A8 to the Signal Generator as follows: connect multipin connector A8P2 to A5A3J2; connect P7, P10 and P11 to A8A1J2, A8A1J4 and A8A1J5, respectively; and connect W2P2 and W3P1 to A8A1J3 and A8A1J1, respectively.

d. Check that the proper voltages are being applied to A8 (refer to Table 4-4).

4-44. Frequency Counter Time Base Accuracy.

a. Set the rear-panel INT TIME BASE switch to 1 sec and press the front-panel EXT COUNT pushbutton.

b. Couple the 10 MHz time base output of an H-P 5245L frequency counter to the front-panel EXT COUNT connector.

c. Adjust trimmer capacitor A8A3A6C8 until the frequency display readout of the Signal Generator indicates 000.000 kHz.

**NOTE**

The Signal Generator top cover should be removed for as short a time as possible when adjusting the frequency of 4 MHz oscillator A8A3A6Q8.

4-45. Band Center Switching.

a. Connect a Tektronix 585 oscilloscope (DC coupled) to A8A1FL6 (BAND CTR CMD).

b. Set the RANGE MHz selector switch to 7.75 to 16 MHz. While observing the oscilloscope, go up and down the 7.75 to 16 MHz frequency range. The voltage on A8A1FL6 should go to zero volts at 10.9000 MHz ±20 kHz going down frequency and should go to approximately +4 volts at 11.1000 MHz ±5 kHz going up in frequency. If not, perform the adjustments of steps d through g.

c. Connect the Tektronix 585 oscilloscope (AC coupled) to A8A1FL7 (BAND CTR PULSE). The output on A8A1FL7 should be a positive pulse when the voltage at A8A1FL6 changes from zero to approximately +4 volts or from approximately +4 volts to zero.

d. Turn trigger adjust potentiometer A8A3A6R2 and hysteresis adjust potentiometer A8A3A6R1 fully clockwise.

e. Set the Signal Generator frequency to 10.9000 MHz. The voltage on A8A1FL6 should be approximately +4 volts. Slowly adjust trigger adjust potentiometer A8A3A6R2 until this voltage goes to zero.

f. Set the Signal Generator frequency to 11.1000 MHz. Slowly adjust hysteresis adjust potentiometer A8A3A6R1 until the voltage on A8A1FL6 goes to +4 volts.

g. Repeat step b.

4-46. Counter Troubleshooting Techniques and Checkout. As with all sophisticated digital electronic equipment, troubleshooting techniques that may be applied to the frequency counter can vary considerably. In the suggested technique, a test frequency is inserted and logic states throughout the counter circuits are monitored and compared with the "normal" states for the test frequency. This signal tracing technique requires a detailed knowledge of the logical operations performed. An oscilloscope is used to monitor the logic states. The theory of operation presented in Section III and in this section describes the logical operations in detail and also provides tables of logic states at selected functional output points for each frequency band.

4-47. Table 4-9 provides a checkout procedure for localizing malfunctions to a printed circuit board level within A8A3. The circuit board may be replaced or additional troubleshooting conducted using the signal tracing technique described above in conjunction with "normal" voltage measurements at transistors, etc., furnished in Table 4-18. Proceed as follows:

a. With A8 removed from the Signal Generator, disassemble A8 as described in steps a through c of paragraph 4-43. Install the printed circuit board to be tested on a board extender.

**NOTE**

The Signal Generator is used as the frequency source for the checkout procedures.

b. If the counter is inoperative on all frequency bands, set the Signal Generator to approximately 248 MHz (the low end of the 248-512 MHz band). The exact frequency is not important. Follow the checkout procedure for an inoperative counter in Table 4-9.

c. If the malfunction exists on two or more bands, but not on all, set the Signal Generator to the low end of an

## 4-48. DETAILED CIRCUIT DESCRIPTION.

4-49. A detailed circuit description for each of the functional blocks of the Signal Generator precedes the respective functional schematic diagram.

4-50 FREQUENCY GENERATION CIRCUITRY. Figure 4-15.

4-51 248 - 512 MHz Master Oscillator. UHF transistor A1A1Q1 is a common-base amplifier with positive feedback. The collector of Q1 is connected to the center conductor of a 1/4-wave length resonant coaxial cavity which determines the frequency of oscillation. The front-panel FREQUENCY control tunes the oscillator over the 248 to 512 MHz frequency range by changing the physical length of the cavity with a movable ceramic slug. Electronic fine tuning (over a range of at least 300 ppm) is achieved by means of varactor A1CR1, which alters the electrical length of the coaxial line by effectively changing the capacitance at the end of the cavity. Loop coupling is employed at the shorted end of the coaxial cavity to extract the master oscillator output power level of approximately 2 milliwatts (+3 dBm).

4-52 Frequency Divider. The following subparagraphs describe the stages of the frequency divider.

4-53 Band 1 Amplifier A2A1. The basic 248 to 512 MHz output of master oscillator A1 is applied through A2P1 and transformer-coupled to both the emitter of A2A1Q1, the first stage of a saturating buffer amplifier, and the emitter of isolation amplifier A2A1Q2. Saturating buffer A2A1Q1 and A2A1Q5 boosts the level of the master oscillator signal to approximately 5 milliwatts, a level sufficient to drive band 2 frequency divider A2A2A1, the first stage of a five stage binary frequency divider chain. In addition to providing both the leveling action and drive for the following binary divider, the saturated buffer amplifier also provides approximately 80 dB of isolation between the first frequency divider and isolation amplifier A2A1Q2, thereby eliminating divider-generated subharmonics from appearing at the output when the RANGE MHz switch is set to 248 - 512 (band 1).

4-54 Band 2 Frequency Divider A2A2A1 and Band 3 Frequency Divider A2A2A2. These two frequency dividers are identical except for frequency-dependent component values. The drive signal from the preceding stage is applied to toggle transistors Q1 and Q2, a high-speed banary divider. The divided frequency output appears at each collector. The output at the collector of Q2 is coupled through a two stage isolation amplifier (Q3 and Q4) which serves a three-fold function: it amplifies the divided signal to a level suitable to drive the following divider stage; it filters the output waveform to provide a relatively clean sinusoidal output; and it provides the necessary isolation to prevent f/2 leakage signals from the following stage.

4-55 Since the output of the master oscillator is greater than one octave and the divider outputs contain harmonic distortion products, low-pass filters with switchable upper cutoff frequencies are placed in the divider output path. Each filter consists of capacitors C1 through C3, inductor L1 and diode CR1. When the output frequency of master oscillator A1 is below the geometric mean of its range (355 MHz), the band center command voltage applied to the base of inverter A2A1Q3 is 0 volts. The transistor is therefore cutoff and switch A2A1Q4 is saturated, causing diode CR1 to conduct. Bridging capacitor C2 is in the circuit and the cutoff frequency of the filter is just above the geometric mean of the band. The filter attenuates unwanted harmonic products of the divided signal developed at the collector of Q1, thereby providing a clean sinusoidal output to drive the modulator.

4-56 Similarly, when the master oscillator output frequency is above the geometric mean, the band center command voltage applied to the base of A2A1Q3 is +5 volts. Switch A2A1Q4 is cutoff, preventing diode CR1 from conducting, thereby removing bridging capacitor C2 from the filter. This action causes the cutoff frequency of the filter to be shifted slightly above the high end of the band, while maintaining a steep skirt, to again provide a clean output waveform for driving the modulator.

4-57 Band 4 Frequency Divider A2A2A3, Band 5 Frequency Divider A2A3A1 and Band 6 Frequency Divider A2A3A2. The 62 to 128 MHz output of the band 3 frequency divider is applied to A2A2A3MC1, an integrated circuit binary divider. One output of the divider is coupled through isolation amplifier A2A2A3Q1 to the band 5 divider while the other output is coupled to A2A1S1. The band 4, 5 and 6 frequency dividers are similar, with the one following exception: the band 6 divider has three outputs. One output is applied to switch A2A1S1, the second output (at A2J3) is coupled to the optional plug-in frequency extender module and the thrid output (at A2J2) is applied to the frequency counter. Note that, unlike the band 2 and 3 frequency dividers, the band 4, 5 and 6 frequency dividers do not have low-pass filters in the output path to switch A2A1S1.

4-58 The output of isolation amplifier A2A1Q2 and the outputs of each subsequent frequency divider, all being typically -10 dBm, are coupled to a high-isolation printed circuit type RF switch, A2A1S1. This switch, whose position is determined by the setting of the RANGE MHz control, routes the output of the band 1 amplifier or any one of the five divider outputs to the following stage.

4-59 BALANCED MODULATOR AND LEVEL CONTROL CIRCUITRY. Figure 4-16.

4-60 Wideband Preamplifier. RF amplifiers A3A2A1Q1 and A3A2A1Q2 increase the frequency divider output (7.75 to 512 MHz) by approximately 15 dB. High-frequency series compensation is provided by coils A3A2A1L2 and A3A2A1L4; low-frequency compensation is provided by capacitors A3A2A1C10 and A3A2A1C14. Degenerative feedback from the emitter of Q2 to the base of Q1 (through R4) provides the wideband preamplifier with a low input VSWR over its operating range. The low input VSWR presents a reasonably constant output impedance to the frequency divider, particularly in bands 2 and 3, where the low-pass filters depend on a 50-ohm load for proper frequency response. The preamplifier provides a minimum saturated output power level of 1 milliwatt (0 dBm) to the first balanced modulator.

4-61 Balanced Modulators. First balanced modulator A3A2A2 and second balanced modulator A3A2A3 are sealed, non-repairable modules with bandpass characteristics similar to the wideband preamplifier. The insertion loss of the two modulators in series can be varied over a dynamic range of approximately 60 dB. The RF impedance of the diodes within the two modulators is varied via the RF level control circuit as described in paragraph 3-23.

4-62 RF Level Control Circuit. The stages of the circuit are discussed in the following subparagraphs.

4-63 Leveling Amplifier A3A1MC2. This stage is an inverting IC operational amplifier which is connected to the output of adding network A3A1R28, A3A1R29 and A3A1C16. The gain of the amplifier is normally determined by feedback network A3A1R32, A3A1C17; and resistors A3A1R28 and A3A1R29. However, during pulsed operation, P-channel FET A3Q10 is gated on by 0 volts (ground) from switching transistor A3A1Q9, thereby connecting resistor A3A1R35 in the amplifier feedback path. This reduces the DC gain of the amplifier.

4-64 Isolation Amplifier A3A1Q11 and Emitter Followers A3A1Q12 and A13A1Q15. Stage A3A1Q11 is a common-emitter amplifier which increases the output of the preceding leveling amplifier to a level suitable to drive the balanced modulators. Emitter followers A3A1Q12 and A3A1Q15 provide a low-impedance path to the balanced modulators.

4-65 Sample and Hold Circuit. The stages of the sample and hold circuit are discussed in the following subparagraphs.

4-66 Inverters A3A1Q2, A3A1Q4 and A3A1Q5. These three common-emitter amplifiers function as switching transistors. When the Signal Generator is set up for external pulse modulation and no positive modulating signal is present at the input of A3A1Q2, both this transistor and A3A1Q5 are cutoff and A3A1Q4 is saturated. This results in a +12 volts output from A3A1Q5. When a positive modulating signal is applied to A3A1Q2, both it and A3A1Q5 are saturated and A3A1Q4 is cutoff. This results in a 0 volts (ground) output from A3A1Q5. When not in pulsed operation, +12 volts from switching transistor A3A1Q3 places A3A1Q4 at saturation and A3A1Q5 at cutoff, resulting in a +12 volts output from A3A1Q5.

4-67 FET A3A1Q6 and Unity-gain Amplifier A3A1MC1. P-Channel FET A3A1Q6 is gated on by the 0 volts output (ground) of inverter A3A1Q5. When gated on, capacitor A3A1C11 is allowed to charge to the negative output of RF detector A5A1A1 via the saturated FET and resistor A3A1R20. A3A1MC1 is a non-inverting IC operational amplifier which is connected in a voltage follower configuration Feedback resistor A3A1R19 is tied to the inverting input terminal of A3A1MC1.

4-68 WIDEBAND POWER AMPLIFIER CIRCUITRY. Figure 4-17

4-69 RF amplifiers A4A3Q1 through Q7 increase the second balanced modulator output (7.75 to 512 MHz) by approximately 50 dB. High-frequency series and shunt compensation and low-frequency compensation are used throughout the amplifier chain to obtain the required bandpass. Degenerative feedback from the emitter of Q2 to the base of Q1 (through R3) provides the wideband power amplifier with a low input VSWR over its operating range. The output power level from power amplifier Q7 is greater than +14 dBm (VX2 pushbutton released) or +20 dBm (VX2 pushbutton pressed).

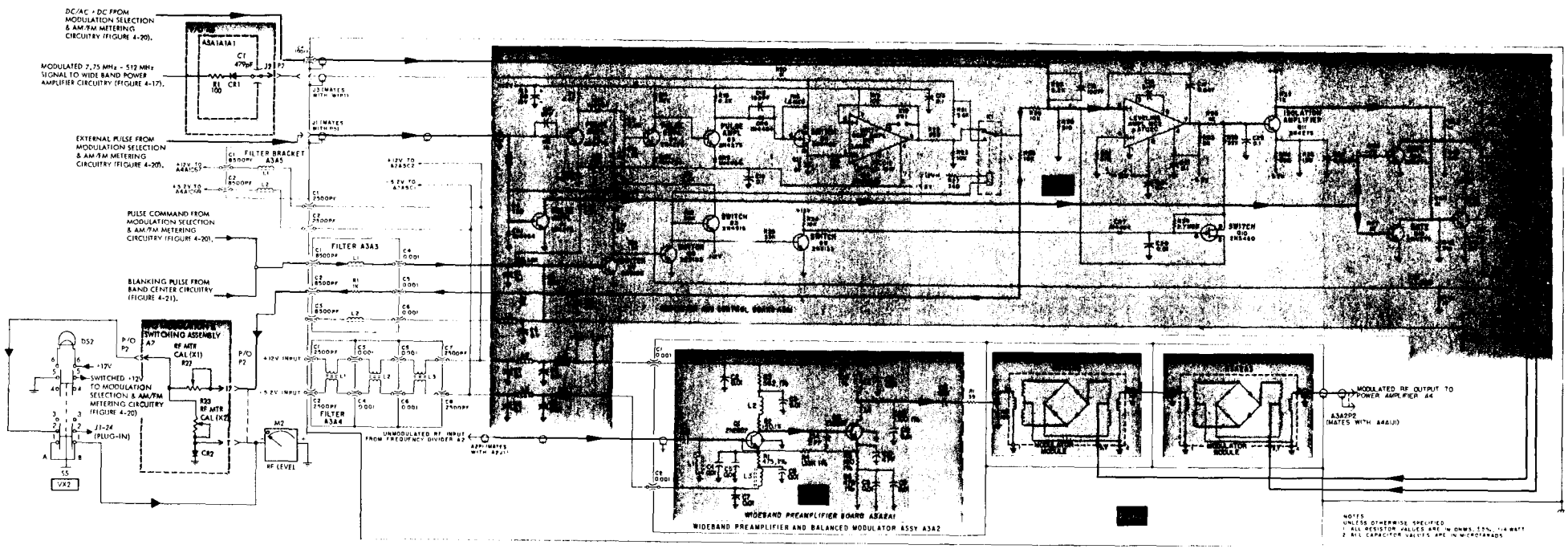
4-70 LOW-PASS FILTER CIRCUITRY. Figure 4-18.

4-71. This circuitry consists of a manually-driven filter selector turret switch (mechanically ganged to the RANGE MHz switch) containing six pairs of low-pass filters, five electronically actuated reed relays, and one magnetically actuated reed relay. When the RANGE MHz switch is set to any position other than PLUG-IN, the output of wideband power amplifier A4 is coupled through A5A1J1 and applied simultaneously to reed relays A5A1K1 and A5A1K3. A band center command voltage, obtained from band center command circuitry (refer to paragraph 4-90) is coupled through R-C RFI filter A5A1A6 to the base of switdh A5A1A2Q1. When the output frequency of master oscillator A1 is below its geometric mean of 355 MHz, the command voltage is 0 volts and switches A5A1A2Q1 and A5A1A2Q2 are both in cutoff. Switch A5A1A2Q3, however, is saturated due to its base being tied to +6 volts through reed relays A5A1K1 and A5A1K2, resistor A5A1A2R3 and diode A5A1A2CR3, energizing reed relays A5A1K3 and A5A1K4 to insert the appropriate low end low-pass filter into the signal path. Note that resistor A5A1A2R3 limits the current flow through relays A5A1K1 and A5A1K2 to a level below that value which is required for energization of the relays. Each low end filter has an extremely sharp skirt at its high frequency limit to sharply attenuate harmonics of the carrier frequency generated either by the frequency divider, modulator or power amplifier.

4-72. Similarly, when the output frequency of master oscillator A1 is above its geometric mean of 355 MHz, the band center command voltage obtained from the frequency counter is +5 volts. This level drives both A5A1A2Q1 and A5A1A2Q2 into saturation, energizing reed relays A5A1K1 and A5A1K2 to insert the appropriate high end low-pass filter into the signal path. Note that saturation of A5A1A2Q2 cuts off A5A1A2Q3 and prevents energization of relays A5A1K3 and A5A1K4. Each high end filter, like each low end filter, has an extremely sharp skirt at its high frequency limit to greatly attenuate unwanted harmonics of the carrier frequency.

4-73. The output of the selected low-pass filter (as determined by the setting of the RANGE MHz switch and the operating frequency of the master oscillator) is simultaneously applied to the RF level detector of the balanced modulator and level control circuitry; and, through an R-C network (A5A1A1R2, A5A1A1C1 and A5A1A1C2) that establishes the 50-ohm source impedance, to the 0-150 dB attenuator circuitry.

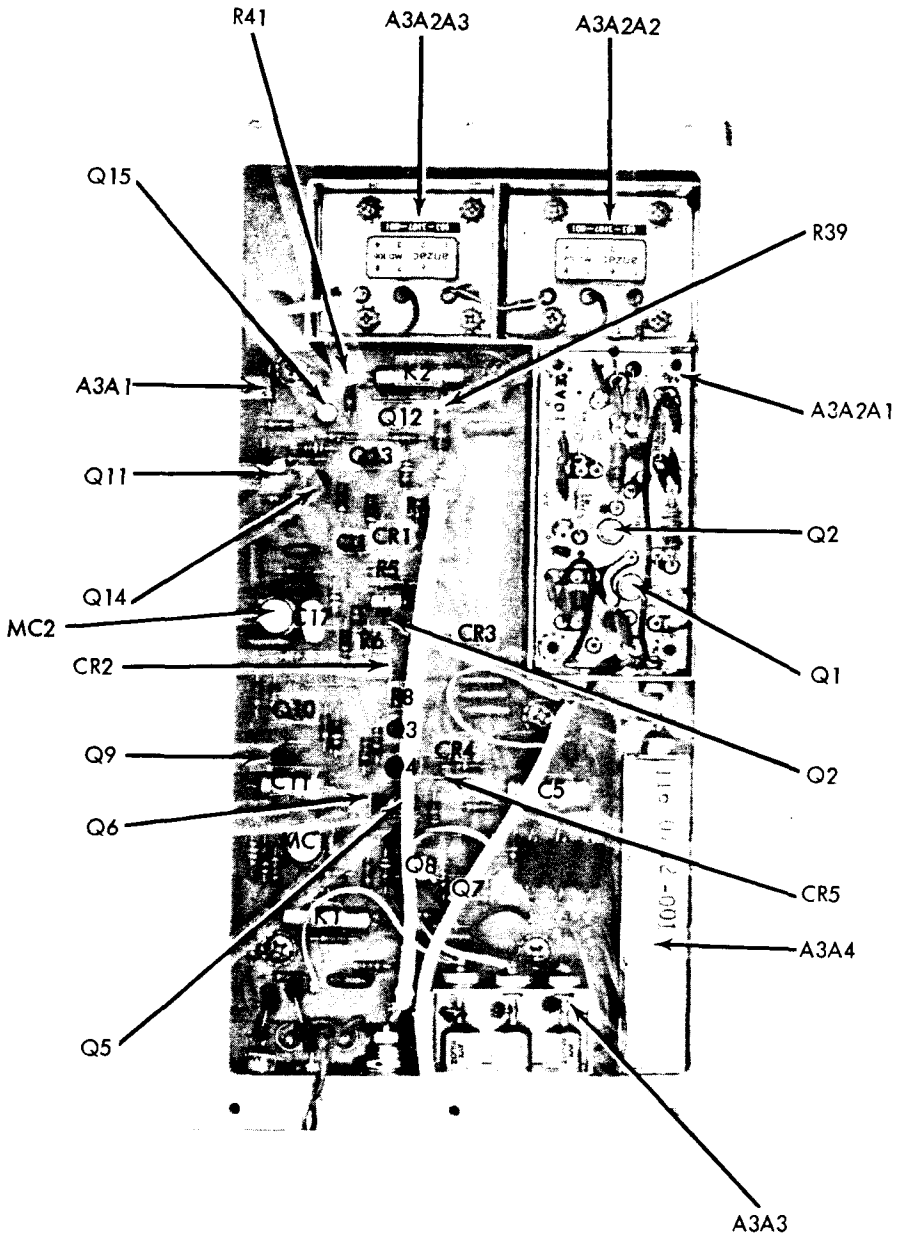
4-74. When the RANGE MHz switch is set to PLUG-IN, a magnet on the rotor of the turret switch is placed in close proximity to reed relay A5A1A1K6. Closure of the relay contacts energizes reed relay A5A1K5, coupling the output of the plug-in frequency extender module to both the RF level detector and the output attenuator. Note that diodes A5A1A2CR1 and A5A1A2CR2 clamp the bases of A5A1A2Q1 and A5A1A2Q3 respectively, at ground. The output of the plug-in module is coupled through A5A1A1R3 (which establishes the plug-in module output impedance at 50 ohms) to both the output attenuator and, via A5A1A1R2, A5A1A1C1 and A5A1A1C2, to the RF level detector.




A3

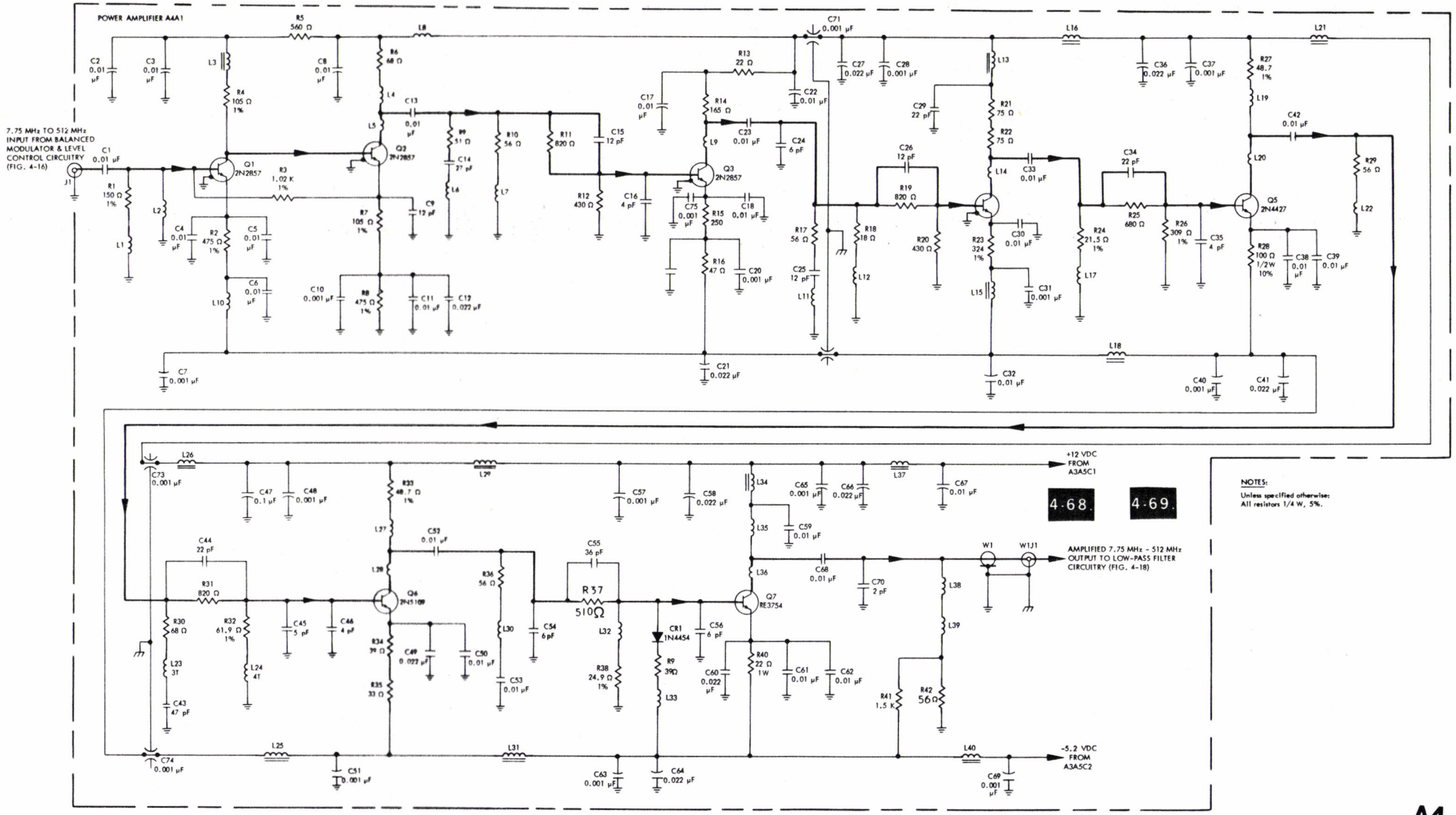
4-16.

Figure 4-16. Balanced Modulator and Level Control Circuitry, Functional Schematic Diagram




# A3

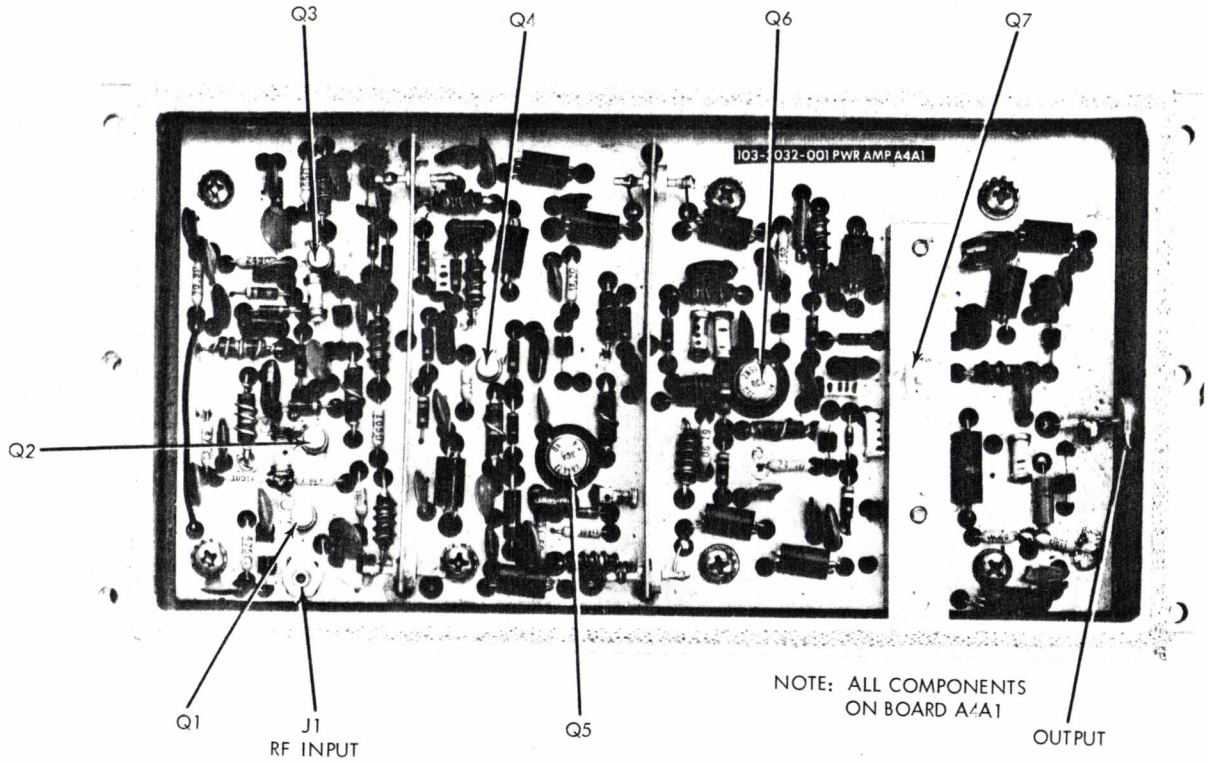
Parts Locations




A4

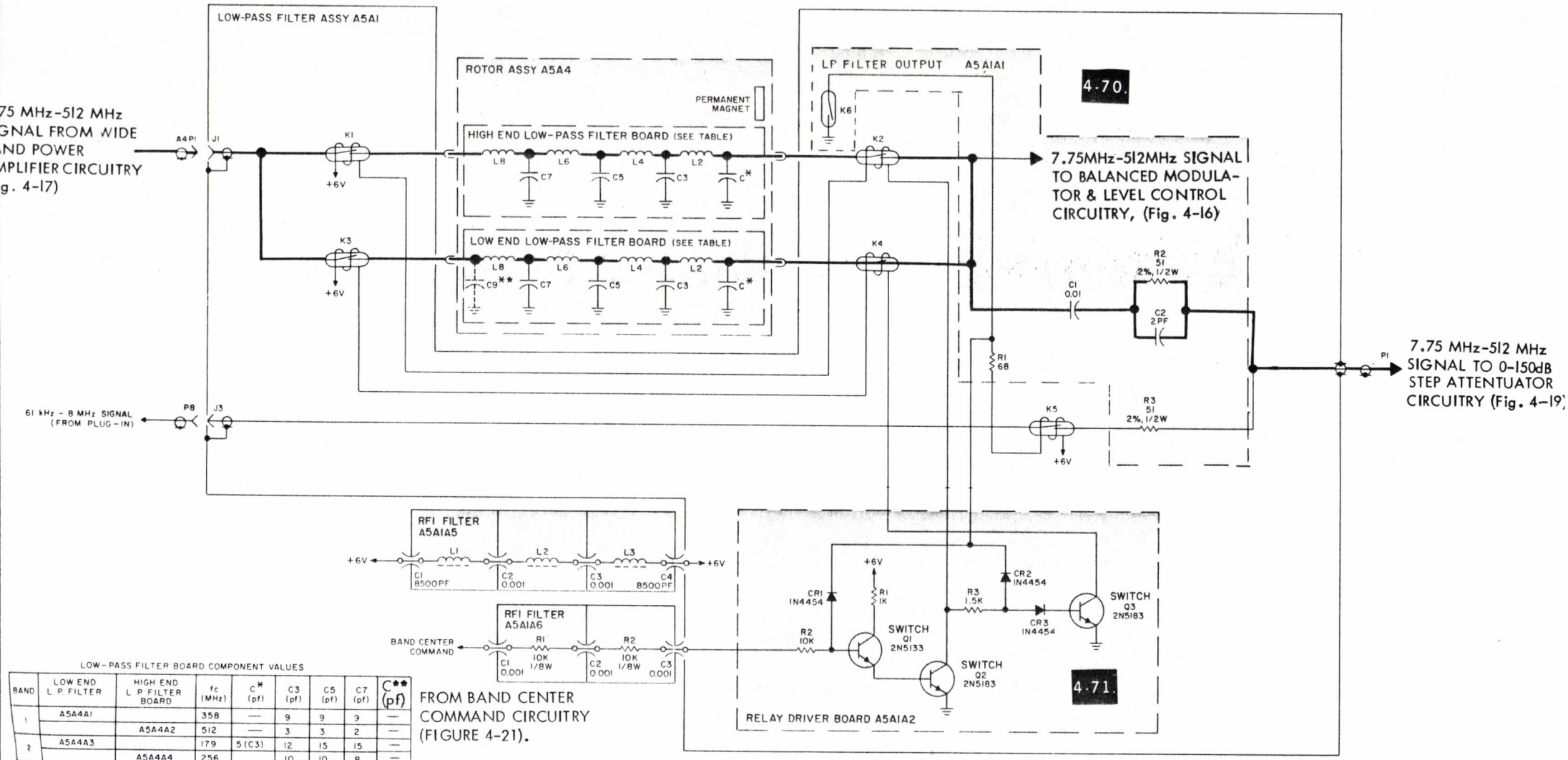
4-17.

Figure 4-17. Wideband Power Amplifier Circuitry, Functional Schematic Diagram




**A4**

Parts Locations




FROM BAND CENTER COMMAND CIRCUITRY (FIGURE 4-21).

LOW-PASS FILTER BOARD COMPONENT VALUES

| BAND | LOW END L.P. FILTER | HIGH END L.P. FILTER BOARD | fc (MHz) | C* (pf) | C3 (pf) | C5 (pf) | C7 (pf) | C** (pf) |
|---|---|---|---|---|---|---|---|---|
| 1 | A5A4A1 | | 358 | — | 9 | 9 | 3 | — |
| | | A5A4A2 | 512 | — | 3 | 3 | 2 | — |
| 2 | A5A4A3 | | 179 | 5 (C3) | 12 | 15 | 15 | — |
| | | A5A4A4 | 256 | | 10 | 10 | 8 | — |
| 3 | A5A4A5 | | 89.5 | 20 (C5) | 33 | 30 | 27 | — |
| | | A5A4A6 | 128 | 15 (C4) | 24 | 22 | 18 | — |
| 4 | A5A4A7 | | 44.75 | 43 (C7) | 68 | 62 | 51 | — |
| | | A5A4A8 | 64 | 30 (C6) | 47 | 43 | 36 | — |
| 5 | A5A4A9 | | 22.37 | 82 (C9) | 130 | 130 | 100 | — |
| | | A5A4A10 | 32 | 56 (C8) | 91 | 91 | 75 | — |
| 6 | A5A4A11 | | 11.187 | 160 C11 | 270 | 240 | 200 | 30 (C12) |
| | | A5A4A12 | 16 | 120 C10 | 180 | 180 | 150 | — |

NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, + 5%, 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
** PARTS OF POTOR ASSEMBLY A5A4
* C9 4 pF A5A4A4



Figure 4-18. Low Pass Filter Circuitry, Functional Schematic Diagram

4-75 0 - 150 dB STEP ATTENUATOR CIRCUITRY. Figure 4-19

4-76 The RF output level of the signal from the low-pass filter circuitry is adjustable over a 16 dB range with dBm continuous control A6A1R1. To provide continuous adjustment of the RF level over a 166 dB range, the 70 dB attenuator control assembly (A6A2) and the 80 dB attenuator control assembly (A6A1) are employed. Assembly A6A2 consists of 10 dB, 20 dB, and 40 dB chip (two 20 dB chips in series) attenuators, which provide up to 70 dB of attenuation, in 10 dB steps. In this attenuator control assembly lamps A6A2A2DS1 through DS3 control the operation of electronic switches A6A2A1Q1 through Q9, via phototransistors A6A2A1PT1 through PT3. Assembly A6A1 consists of four 20 dB chips, a total of 80 dB which is inserted in one step. In this attenuator control assembly, lamp A6A1A1DS1 controls the operation of electronic switches A6A1A2Q1 through Q6, via phototransistor A6A1A2PT1. The desired attenuation, from 0 to 150 dB, is obtained by inserting and bypassing various combinations of the 10, 20 40 and 80 dB attenuators as indicated in Table 3-1 and described in paragraph 3-37.

4-77 MODULATION SELECTION AND AM/FM METERING CIRCUITRY. Figure 4-20

4-78 RF Level Set Network. This resistive network consisting of A7R1, A7R3, A7R5 and A6A1R1 provides a DC level output which represents the average power of the RF output. During AM operation, an AC signal is added to this DC level. The level set network operates as follows. When in CW, FM or pulsed operation, resistor A7R5 is returned to ground through the released AM INT and AM EXT pushbuttons. With the VX2 pushbutton in the released position, the +12 volts DC applied to A7R3 results in approximately a +4 volts output from the RF level set network is applied to the balanced modulator and level control circuitry (paragraph 4-59). When the VX2 pushbutton is pressed, switched +12 volts is applied to the junction of A7R1 and A7R3, effectively shorting output A7R3. This results in a 0 to +8 volts output from the RF level set network. During AM operation, the AC signal developed across the AM LEVEL control is added to the DC level at the junction of A7R5 and A7R6. Factory-selected resistor A7R7 places the summing point at DC ground.

4-79 1 kHz Oscillator. The following subparagraphs describe the stages of the 1 kHz oscillator.

4-80. AGC Amplifier A7A1. This stage is an inverting IC operational amplifier which is disabled by the negative DC voltage at its inverting terminal (pin 2), when the AM INT and FM INT pushbuttons are both in the released position. Under this condition, a positive DC output is obtained from the amplifier. When either the AM INT or FM INT pushbutton is pressed, +12 volts is applied to the junction of A7R85 and A7R24. The resulting positive DC voltage at the inverting terminal of the amplifier enables it. Under this condition, a negative DC output is obtained from the AGC amplifier.

4-81. FET A7Q2. This P-channel FET is normally held at cutoff by the positive DC output of the AGC amplifier. When the AM INT or FM INT pushbutton is pressed, the negative DC output of the AGC amplifier gates the FET on. The FET then acts as a variable resistor under the control of the applied negative DC signal from A7A1.

4-82. Oscillator A7A2 and Filter A7A3. Stage A7A2 employs an IC operational amplifier in a Wien bridge oscillator configuration. With FET A7Q2 at cutoff, the feedback network at the inverting terminal (pin 2) of A7A2 is principally composed of A7R35 and A7R32. Under this condition, the oscillator is disabled. When the FET is gated on, A7C8 and the FET are bridged across A7R32, causing the oscillator to be enabled. Rear panel INT MOD ADJ screwdriver control R3 varies the resistance of the R-C phase shifting network at the non-inverting terminal (pin 3) of A7A2, thus varying the oscillator frequency ±2 percent of 1 kHz. The oscillator output is coupled through active IC filter network A2A3 to the front panel MOD OUT 1 kHz connector and the AM LEVEL or FM DEV control. Any variation in the oscillator output is sensed by peak detector A7CR5 and A7C7, and applied to the non-inverting terminal (pin 3) of AGC amplifier A7A1. The resulting output of A7A1 then controls the resistance of the FET in such a manner as to return the output level of the 1 kHz oscillator to the proper value (2.0 volts peak-to-peak, nominal).

4-83 FM Amplifier. This stage consists of difference amplifier A7Q3/Q4 and output amplifier A7Q6. When in internal or external FM operation, the FM input is coupled through A7Q3A to the base of A7Q4A. At this time, the vernier/AFC output of the frequency lock circuitry (paragraph 4-127) is coupled through A7Q3B to the base of A7Q4B. The resulting output at the collector of A7Q4B is routed through output amplifier A7Q6 to the master oscillator varactor (via the pressed FM INT or FM EXT pushbutton).

4-84 AM Metering Circuit. This circuit comprises a buffer amplifier and an AC detector. Stage A7Q1, a common-emitter amplifier, isolates the succeeding AC detector from the internal 1 kHz oscillator and external AM circuits. Diode A7CR1 and capacitor A7C5 provide peak detection of the AM signal. The peak detected output is routed through resistor A7R13 and % AM cal potentiometer A7R14 to the % AM/FM DEV meter, when the AM/FM switch is set to AM.

4-85 FM Metering Circuit. The following subparagraphs describe the stages of the FM metering circuit.

4-86. FM Metering Buffer A7A4. This stage is a non-inverting IC operational amplifier (with a gain of approximately 6) which provides isolation for the FM peak deviation metering outputs.

4-87. Range Buffer A7A3. This stage is a non-inverting IC operational amplifier (with a gain of approximately 80) which isolates the meter multipler networks (A7R15-R21; and A7S7-S10) from the succeeding AC detector.

4-88. AC Detector A7A6. This stage is a non-inverting IC operational amplifier which peak detects the negative alternation of the applied AC signal. Diode A7CR10 and capacitor A7C35 provide peak detection of the signal. The feedback loop to the inverting input terminal of A7A6 is closed by A7CR9 for the positive alternation of the AC signal,

thereby preventing damage to A7A6. Similarly, the feedback loop to the non-inverting input terminal is closed by the diode detector and the succeeding DC amplifier stage for the negative alternation of the AC signal.

4-89. DC Amplifier A7A7. This stage is an inverting IC operational amplifier which amplifies the peak detected output of A7A6 sufficiently to obtain full-scale calibrated readings on the % AM/FM DEV meter for the 30-, 100-, 300- and 1000-kHz FM peak deviation ranges provided by the FM RANGE (kHz) pushbuttons. Potentiometer A7R72 provides electrical zeroing for the FM deviation scales of the % AM/FM DEV meter. FM dev meter cal potentiometer A7R77 provides an adjustment for the 100 kHz FM peak deviation metering output.

4-90. BAND CENTER COMMAND CIRCUITRY. Figure 4-21.

4-91. Amplifier/Limiter A8A3A6Q6 and A8A3A6Q5. This circuit is a two-stage capacitor-coupled amplifier. Each stage is a common-emitter amplifier. Diodes A8A3A6CR4 and CR2 limit the positive and negative swings of the 7.75 to 16 MHz signal applied to the succeeding low-pass filter.

4-92. Low-pass Filter. This circuit is L-type filter consisting of capacitor A8A3A6C3 and inductor A8A3A6L1. The characteristics of the low-pass filter are such that its insertion loss is approximately 5 dB at 11.093 MHz, which corresponds to the geometric mean (355 MHz) of the master oscillator tuning range.

4-93. Detector. Diode A8A3A6CR1 and the R-C network composed of capacitor A8A3A6C2 and resistor A8A3A6R6 peak detect the negative alternation of the low-pass filter output signal. Potentiometer A8A3A6R2 adjusts the DC bias level on which the detector output rides.

4-94. Schmitt Trigger A8A3A6Q1 and A8A3A6Q2. When the signal applied to the low-pass filter is below the geometric mean of the master oscillator tuning range, the negative output of detector A8A3A6CR1 causes A8A3A6Q1 to be turned off and A8A3A6Q2 to be turned on. Under this condition, the output of A8A3A6Q2 is approximately +2 volts DC. When the signal applied to the low-pass filter is at or above the geometric mean, the detector output goes positive (by virtue of the 5 dB insertion loss of the low-pass filter and the positive DC voltage from A8A3A6R2), thereby causing the Schmitt trigger to change state. Under this condition, the output of A8A3A6Q2 is +5 volts DC. Potentiometer A8A3A6R1 adjusts the hysteresis of the Schmitt trigger so that triggering occurs at 11.10 MHz when tuning up in frequency and 10.90 MHz when tuning down.

4-95. Gates A8A3A6Q3 and A8A3A6Q4. These gates convert the Schmitt trigger outputs to the TTL logic levels required by the succeeding delay logic circuit. The output of gate A8A3A6Q4 is a logical ZERO level (0 volts DC nominal) for frequencies below the geometric mean and a logical ONE level (+5 volts DC nominal) for frequencies equal to or above the mean.

4-96. Delay Logic Circuit. This circuit comprises monolithic, TTL, inverters in A8A3A6IC1 and two-input AND/OR invert gates in A8A3A6IC2. The output of gate A8A3A6Q4 is coupled through two inverters in IC1 to provide the band center command level (see Figure 4-22). The gate A8A3A6Q4 output is also applied to the remainder of the delay logic circuit, which provides a trigger pulse of approximately 2.25 microseconds to the output monostable multivibrator (one-shot). The R-C network composed of A8A3A6R17 and A8A3A6C9 determines the pulse width of the trigger pulse.

4-97. Monostable Multivibrator A8A3A6IC3. This monolithic TTL one-shot provides a positive output pulse which blanks the RF output (via the balanced modulator and level control circuitry) for the time required to switch low-pass filters in assemblies A2 and A5. Capacitor A8A3A6C7 and an internal timing resistor (2 kilohms nominal) in A8A3A6IC3 set the output pulse width at approximately10 milliseconds.

4-98. FREQUENCY COUNTER PRE-SCALER CIRCUITRY. Figure 4-23.

4-99. Amplifier A8A3A4Q1. This stage is a capacitor-coupled, common-emitter amplifier. Diode A8A3A4CR1 amplitude limits the negative alternation of the applied 7.75 to 16 MHz squarewave signal from the frequency generation circuitry (refer to paragraph 4-50).

4-100. Frequency Divider A8A3A4IC1-IC3. This circuit comprises three monolithic, TTL, D-type flip-flops in cascade. Each of these edge-triggered flip-flops functions as a binary divider. During external count operation, the internal/external selector logic applies a logical ZERO level to the clear input of the first flip-flop. This input disables the frequency divider.

4-101. Emitter Follower A8A3A4Q2, Amplifier A8A3A4Q3, and Emitter Follower A8A3A4Q4. Stage A8A3A4Q2 provides a low impedance path to amplifier A8A3A4Q3. This emitter follower also isolates external circuits (which are coupled to the EXT COUNT connector) from succeeding circuits. Amplifier A8A3A4Q3 is a capacitor-coupled, common-emitter amplifier. Diode A8A3A4CR2 amplitude limits the negative alternation of the external count signal. Emitter follower A8A3A4Q4 isolates the amplifier from the succeeding TTL logic circuits.

4-102. Pulse Shaper. This Schmitt trigger employs two of the monolithic, TTL inverters in A8A3A4IC5. The resulting 0V to +5V squarewave output of the pulse shaper is applied to the internal/external count selector logic.

4-103. Pre-scaled Frequency Selector Logic. This logic comprises the following monolithic, TTL gates in A8A3A4IC7: four, dual-input AND gates and an OR invert gate. One of three frequency divider outputs ($F_O/8$, $F_O/16$, or $F_O/32$) or the external count signal is selected by the pre-scaled frequency

4-151. OUTPUT ATTENUATOR A6.

4-152. 0-80 dB Step Attenuator A6A1.

a. Loosen and remove the seven screws that secure the brace to the low-pass filter assembly, main chassis mounting block, and side of plug-in housing. Withdraw the brace from the main chassis.

b. Disconnect A5A5P1 from A6A1AT1J1.

c. Loosen and remove four screws that secure A6A1 to the main chassis bottom plate.

d. Unscrew the coaxial connection which interconnects A6A1 and A6A2.

e. Unsolder the black, white/grey, and blue leads at the GRD and E1 eyelets of A6A1 and the RFI filter, respectively.

f. Carefully withdraw A6A1 from the main chassis.

4-153. 0-70 dB Step Attenuator A6A2.

a. Perform steps a through d of paragraph 4-152.

b. Loosen and remove the four screws that secure A6A2 to the main chassis bottom plate.

c. Unsolder the two coaxial cables from the wiper and end terminals of A6A1R1. Note that one of these cables. terminates at J1-15 and the other at A3C3. Unsolder the remaining coaxial cable from the grounded terminal of A6A1R1. This cable is terminated at P2-P. Unsolder the ground leads of these three cables from the ground lug.

d. Unsolder the blue lead from A6A2 RFI filter. Unsolder the black ground lead from the lug on the filter.

e. Carefully remove A6A2 from the main chassis.

4-154. MODULATION AND SWITCHING ASSEMBLY A7.

a. Remove frequency counter A8 as described in paragraph 4-155.

b. Loosen and remove the five screws that secure A7 to the main chassis bottom plate.

c. Disconnect multipin connector P2 from A7J1.

d. Carefully lift A7 from Signal Generator.

4-155. FREQUENCY COUNTER A8 .

a. Remove the screw that secures the counter box assembly rear support strut to the main chassis bottom plate.

b. Disconnect multipin connector A8P2 from A5A3J2.

c. Disconnect P7, P10 and P11 from A8A1J2, A8A1J4 and A8A1J5, respectively.

d. Disconnect W2P2 and W3P1 from A8A1J3 and A8A1J1, respectively.

e. Remove the two screws that secure the counter box assembly to the upper lip of the front panel.

f. Carefully slide the counter assembly back and withdraw it from the Signal Generator.

4-156. POWER SUPPLY A9.

a. Loosen and remove the four screws that secure the power supply to the main chassis bottom plate.

b. Disconnect snap-on leads from Q1 and Q2 on rear panel of equipment frame. Tag leads to facilitate reassembly.

c. Disconnect AC power multipin connector from A9J1.

d. Carefully lift the assembly from the Signal Generator. To gain access to components on board subassemblies A9A1 and A9A2 (see Figure 4-2), proceed as directed in steps e through h.

e. Remove four screws that secure protective plate (covers A9A1) to assembly A9. Slide plate off A9.

f. Remove two screws which secure A9A1 to assembly A9.

g. Disconnect leads from filter capacitor A9C1 by removing two screws.

h. Lift A9A1 and A9A2 from A9 and remove A9A2 from connector on A9A1.

## 4-157. VOLTAGE MEASUREMENTS.

4-158. The voltage measurements for the assemblies of the Signal Generator are listed in Tables 4-12 through 4-19. The general conditions for voltage measurements are:

a. All voltages measured with respect to chassis (grd) using VTVM.

b. RANGE MHz and FREQUENCY control set for 8.0 MHz (approximately).

c. Unless other wise specified:

1. All pushbuttons released.

2. All controls set to approximate mid-range.

3. Counter in the normal (unlocked) mode.

d. For full Reference Designator, put Assembly Number in table heading before listed Reference Designator.

TABLE 4-12. VOLTAGE MEASUREMENTS, FREQUENCY DIVIDER, A2

| Reference Designation | Transistor Type | Terminal Voltage | | |
|---|---|---|---|---|
| | | Emitter | Base | Collector |
| A1Q1 | 2N5180 | - .7 | 0 | + 8.6 |
| Q2 | A473 | - .7 | 0 | + 8 |
| Q3 | 2N5133 | 0 | 0 | +10.4 |
| Q4 | 2N5183 | +10.6 | +10.4 | +12 |
| Q5 | 2N5179 | - .85 | 0 | +12 |
| A2A1Q1 | 2N5179 | + 1.7 | + 2.4 | +10.2 |
| Q2 | 2N5179 | + 1.7 | + 2.4 | +10.2 |
| Q3 | A473 | + 1 | + 1.7V | + 9.2 |
| Q4 | 2N4121 | + 2.6 | + 9.2 | + 9.8 |
| A2A2Q1 | 5179 | + 1.7 | + 2.4 | +10V |
| Q2 | 5179 | + 1.7 | + 2.4 | +10V |
| Q3 | A473 | 1 | + 1.7V | + 9.3V |
| Q4 | 2N4121 | + .5V | + 9.3 | +10V |
| A2A3Q1 | A473 | - 4.2 | - 3.4 | - 1.5 |
| A3A1Q1 | 2N4916 | - 2 | - 2.5 | - 4 |
| A3A2Q1 | 2N5180 | - 4.2 | - 3.6 | - .7 |





TABLE 4-13. VOLTAGE MEASUREMENTS, MODULATOR A3

| Reference Designation | Transistor Type | Terminal Voltage | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Emitter | | Base | | | Collector | | |
| A1Q1 | 2N4275 | 0 | | 0 | | | .02 | | |
| A1Q2 | 2N4275 | - .25 | | 0 | | | + 7.7 | | |
| A1Q3 | 2N4916 | 12 | | 11.2 | | | 11. | | |
| A1Q4 | 2N4275 | - 4.4 | | - 3.6 | | | - 4.3 | | |
| A1Q5 | 2N4275 | - 4.7 | | - 4.3 | | | 11.8 | | |
| A1Q6 | 2N5468 | (S) | | (G) 11.4 | | | (D) -1.6 | | |
| A1Q7 | 2N5183 | 0 | | .01 | | | 6 | | |
| A1Q8 | 2N5183 | 0 | | .7 | | | .02 | | |
| A1Q9 | 2N5133 | 0 | | .02 | | | 12 | | |
| A1Q10 | 2N5460 | (S) .005 | | (G) 11.5 | | | (D) .52 | | |
| A1Q11 | 2N4275 | .33 | | .39 | | | 3.04 | | |
| A1Q12 | 2N5179 | .25 | | 1 | | | 0 | | |
| A1Q13 | 2N4275 | 0 | | 0 | | | 1 | | |
| A1Q14 | 2N4275 | 0 | | 0 | | | 1 | | |
| A1Q15 | 2N5179 | .3 | | 1.06 | | | 0 | | |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| MC1 | | 0 | .0005 | 0 | -5.2 | 0 | 0 | 12 | 0 |
| MC2 | | 0 | * | 0 | -5.2 | 0 | 0 | .502 | 12 |
| A2A1Q1 | 2N2857 | - .7 | | 0 | | | 5.4 | | |
| A2A1Q2 | 2N2857 | 4.65 | | 5.4 | | | 10.8 | | |

* Voltage varies with VERNIER attenuator setting.

TABLE 4-14. VOLTAGE MEASUREMENTS, POWER AMPLIFIER A4

| Reference Designation | Transistor Type | Terminal Voltage | | |
|---|---|---|---|---|
| | | Emitter | Base | Collector |
| A1Q1 | 2N2857 | -0.7 | 0 | + 6 |
| A1Q2 | 2N2857 | +5.2 | +6 | +11 |
| A1Q3 | 2N2857 | -0.7 | +0.02 | + 9.6 |
| A1Q4 | 2N2857 | -0.7 | +0.03 | +10 |
| A1Q5 | 2N4427 | -1.6 | -1 | +10.4 |
| A1Q6 | 2N5109 | -0.8 | -0.03 | + 9 |
| A1Q7 | RE3754 | -2.4 | -1.7 | +12 |

TABLE 4-15. VOLTAGE MEASUREMENTS, LOW PASS FILTER A5

| Reference Designation | Transistor Type | | Terminal Voltage | |
|---|---|---|---|---|
| | | Emitter | Base | Collector |
| A1A2Q1 | 2N5133 | 0 | 0 | 6 |
| A1A2Q2 | 2N5183 | 0 | 0 | 5.5V |
| A1A2Q3 | 2N5183 | 0 | .5V | .7 VDC |



TABLE 4-16. VOLTAGE MEASUREMENTS, ATTENUATOR A6

| Reference Designation | Transistor Type | Terminal Voltage* | | |
|---|---|---|---|---|
| | | Emitter | Base | Collector |
| A1A2PT1 | FPT100 | 0 | + .5 | + .15 |
| Q1 | 2N5133 | 0 | + .09 | +5.3 |
| Q2 | 2N5133 | 0 | + .09 | +5.3 |
| Q3 | 2N4916 | +6 | +5.4 | + .5 |
| Q4 | 2N5916 | +6 | +5.4 | + .5 |
| Q5 | 2N4916 | +6 | +5.2 | +5.9 |
| Q6 | 2N4916 | +6 | +5.2 | 5.9 |
| A2A1PT1 | FPT100 | 0 | + .5 | + .15 |
| PT2 | FPT100 | 0 | + .5 | + .15 |
| PT3 | FPT100 | 0 | 0 | + .65 |
| Q1 | 2N5133 | 0 | + .09 | +5.3 |
| Q2 | 2N5133 | 0 | + .09 | +5.3 |
| Q3 | 2N5133 | 0 | + .67 | 0 |
| Q4 | 2N4916 | +6 | +5.4 | + .5 |
| Q5 | 2N4916 | +6 | +5.4 | + .5 |
| Q6 | 2N4916 | +6 | +5.2 | +5.8 |
| Q7 | 2N4916 | +6 | +5.2 | +5.9 |
| Q8 | 2N4916 | +6 | +5.2 | 5.9 |
| Q9 | 2N4916 | +6 | -5.8 | 0 |

* All voltages measured with dBm switch set at +10/1.0V position.

TABLE 4-17. VOLTAGE MEASUREMENTS, MODULATION AND SWITCHING ASSEMBLY A7

| Reference Designation | Transistor Type | Terminal Voltage | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Emitter | | | Base | | Collector | | |
| Q1 | 2N5133 | 3.23 | | | 3.89 | | 7.00 | | |
| Q2 | 2N5460 | (S) 0 | | | (G) 3.2 | | (D) -4.8 | | |
| Q3 | 2N5255 | A -.31 | B -.27 | | A -.74 | B -.66 | A -25.9 | B -25.9 | |
| Q4 | 2N5255 | A .264 | B .264 | | A -.31 | B -.27 | A -25.9 | B -25.2 | |
| Q6 | 2N3645 | -25.8 | | | -25.2 | | -10 | | |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| A1 | | -5.2 | -.07 | 0 | -5.26 | -4.09 | 11.3 | 11.9 | 11.3 |
| A2 | | -10.5 | 0 | 0 | -11.8 | -10.5 | 0 | 11.9 | -.52 |
| A3 | | -10.5 | 0 | 0 | -11.8 | -10.6 | 0 | 11.9 | -.54 |
| A4 | | 0 | 0 | 0 | -5.2 | 3.27 | .679 | .002 | 11.97 |
| A5 | | 0 | 0 | 0 | -5.26 | 3.33 | .517 | .16 | 11.97 |
| A6 | | 0 | -.025 | -.025 | -5.26 | 3.54 | .65 | .03 | 11.97 |
| A7 | | -3.95 | 0 | 0 | -5.26 | -4.05 | .003 | 11.97 | -.52 |

All measurements made in CW +20 dB





TABLE 4-18. VOLTAGE MEASUREMENTS, FREQUENCY COUNTER A8

| Reference Designation | Transistor Type | Terminal Voltage | | |
|---|---|---|---|---|
| | | Emitter | Base | Collector |
| A3A4Q1 | 2N5134 | 0 | + 0.6 | + 2 |
| A3A4Q2 | 2N3904 | + 1.6 | + 2.2 | + 4.7 |
| A3A4Q3 | 2N3904 | + 0.1 | + 0.8 | + 3.4 |
| A3A4Q4 | 2N5087 | + 0.8 | + 0.2 | 0 |
| A3A5Q1 | 2N5088 | + 0.3 | + 0.9 | + 2.7 |
| A3A5Q2 | 2N5087 | + 0.8 | + 0.2 | 0 |
| A3A6Q1 | 2N5133 | + 1 | + 0.3 | + 3 |
| A3A6Q2 | 2N5133 | + 2 | + 2.6 | + 2.6 |
| A3A6Q3 | 2N4916 | + 5 | + 4.1 | + 0.8 |
| A3A6Q4 | 2N5183 | 0 | + 0.8 | + 0.02 |
| A3A6Q5 | 2N5183 | + 0.5 | + 0.9 | + 1.6 |
| A3A6Q6 | 2N5130 | + 1.8 | + 2 | + 3 |
| A3A7Q1 | 2N4916 | 0 | + 2.1 | -25.7 |
| A3A7Q2 | 2N5471 | (S) -10.1 | (G) -10 | (D) -10 |
| A3A7Q3 | 2N4916 | 0 | + 2.2 | -23.8 |
| A3A7Q4 | 2N5471 | (S) -26 | (G) - 0.5 | (D) -10.1 |
| A3A7Q5 | 2N5460 | (S) -26 | (G) -24.3 | (D) -26 |
| A3A7Q6 | 2N5460 | (S) -11.5 | (G) -10.3 | (D) -26 |
| A3A7Q7 | 2N4916 | 0 | - 0.7 | - 0.05 |

TABLE 4-19. VOLTAGE MEASUREMENTS, POWER SUPPLY A9

| Reference Designation | Transistor Type | Terminal Voltage | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Emitter | | Base | | Collector | | | |
| Q1 | 2N4919 | -26.9 | | -26.3 | | -42.6 | | | |
| Q2 | 2N5296 | 5.8 | | 6.4 | | 8.7 | | | |
| Q3 | 2N5296 | 6.4 | | 7. | | 9.6 | | | |
| Q4 | 2N4901 | 17.7 | | 16.9 | | 12.5 | | | |
| Q5 | 2N3059 | -10.5 | | - 9.8 | | - 5.8 | | | |
| A2Q2 | 2N3638A | - 8.4 | | -26.9 | | -27.5 | | | |
| A2Q3A | 2N5255 | - 5.6 | | - 6.3 | | -26 | | | |
| A2Q3B | 2N5255 | - 5.6 | | - 6.2 | | -27.5 | | | |
| A2Q5 | 2N4030 | -26.3 | | -27.5 | | -42.6 | | | |
| A2Q7 | 2N2219A | 12.5 | | 13.1 | | 16.9 | | | |
| A2Q8 | 2N5133 | 12.3 | | 12.5 | | 13.1 | | | |
| A2Q10 | 2N4030 | - 5.8 | | - 6.4 | | - 9.8 | | | |
| A2Q11 | 2N5087 | - 5.6 | | - 5.8 | | - 6.4 | | | |
| A2Q15 | 2N5133 | 5.1 | | 5.3 | | 6.4 | | | |
| A2Q17 | 2N5133 | 6.3 | | 6.4 | | 7 | | | |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| A2IC1 | | -11.1 | .015 | .014 | -12.3 | NC | 6.3 | 11.8 | 5.7 |
| A2IC2 | | -10.9 | .02 | .02 | -12.3 | NC | 6.4 | 11.8 | 5.7 |
| A2IC3 | | -11.2 | .02 | .02 | -12.3 | NC | 6.6 | 12.1 | 6.1 |
| A2IC4 | | -11.1 | 6.02 | 6.02 | -12.3 | NC | 7.0 | 12.1 | 6.7 |
| Q1 Rear Panel | 2N4901 | 9.4 | | | 8.7 | | 5.8 | | |
| Q2 Rear Panel | 2N4901 | 9.4 | | | 8.7 | | 5.8 | | |





## 4-159. ALIGNMENT AND CALIBRATION.

4-160. The adjustments required for the alignment and calibration of the Signal Generator (exclusive of the power supply and the frequency counter) are located on modulation and switching assembly A7. To gain access to the adjustments on assembly A7, remove the left side panel. The location of the adjustments on A7 are shown in Figure 4-13.

**NOTE**

Allow the Signal Generator a 30-minute warmup period before performing the alignment and calibration procedures.

4-161. CALIBRATING RF LEVEL METER.

**NOTE**

Before calibrating the RF LEVEL meter, check that it is mechanically zeroed. If necessary, adjust the pointer mechanical zero positioning screw (located below the meter).

a. Set the front-panel controls as indicated below.

| Control | Setting |
|---|---|
| POWER | Pressed |
| dBm Selector Switch | +10/1.0V |
| dBm Vernier Level | Fully Clockwise |
| VX2 | Released |
| CW | Pressed |
| AM/FM | AM |
| EXT COUNT | Released |
| RANGE MHz | 62 - 128 |
| FREQUENCY | 100 MHz |
| VERNIER Frequency | Mid-range |
| AM LEVEL | Fully Clockwise |
| FM DEV | Fully Clockwise |
| Remaining Controls | As Desired |

b. Connect a General Microwave 421C/454A thermistor mount/power meter to the RF OUT connector via a calibrated 20 dB, 50Ω pad.

c. Adjust the front-panel dBm vernier level control until the General Microwave 454A power meter indicates -6 dBm (which corresponds to +14 dBm at the RF OUT connector).

d. With the VX2 pushbutton released, adjust RF mtr cal (X1) potentiometer A7R22 for a full-scale reading (+4 dB) on the RF LEVEL meter.

e. Press the VX2 pushbutton and adjust the dBm vernier level control, as necessary, until the General Microwave 454A power meter indicates 0 dBm (which corresponds to +20 dBm at the RF OUT connector).

f. With the VX2 pushbutton pressed, adjust RF mtr cal (X2) potentiometer A7R23 for a full-scale reading (+4 dB) on the RF LEVEL meter.

g. Release the VX2 pushbutton. The RF LEVEL meter should indicate +4 dB. If not, repeat steps c through g.

4-162. CALIBRATING % AM/FM DEV METER.

**NOTE**

Before calibrating the % AM/FM DEV meter, check that it is mechanically zeroed. If necessary, adjust the pointer mechanical zero positioning screw (located below the meter).

a. Set the front-panel controls as indicated in step a of paragraph 4-161, except set the Signal Generator frequency to 25 MHz.

b. Connect a Tektronix 585 oscilloscope to the RF OUT connector, via a Narda 20 dB pad.

c. Press the AM INT pushbutton, and adjust the AM LEVEL control for a 100% AM display on the oscilloscope (2 or 3 cycle presentation with a peak-to-peak amplitude of 4 cm and a trough-to-trough amplitude of 0 cm).

d. Adjust % AM cal potentiometer A7R14 for a full-scale reading (100% AM) on the % AM/FM DEV meter.

e. Set the Signal Generator frequency to 100 MHz and press the FM EXT pushbutton.

f. Connect a Hewlett-Packare 3450A DC digital voltmeter to test point A7TP3. Adjust FM cal volts potentiometer A7R80 to obtain a digital voltmeter reading of +0.338 volts ±1 millivolt.

g. With the FM EXT pushbutton in the pressed position, press the FM CAL push-to-operate control and while holding it pressed, rotate the control fully ccw. Note the reading on the frequency counter display. Then, carefully adjust the FM CAL control until the frequency counter display reading increases .100. Carefully release the FM CAL control.

h. Couple a Singer Model SA-70 Spectrum Analyzer to the RF OUT connector.

i. Set the AM/FM switch to FM and press the 100 pushbutton of the FM RANGE (kHz) pushbuttons.

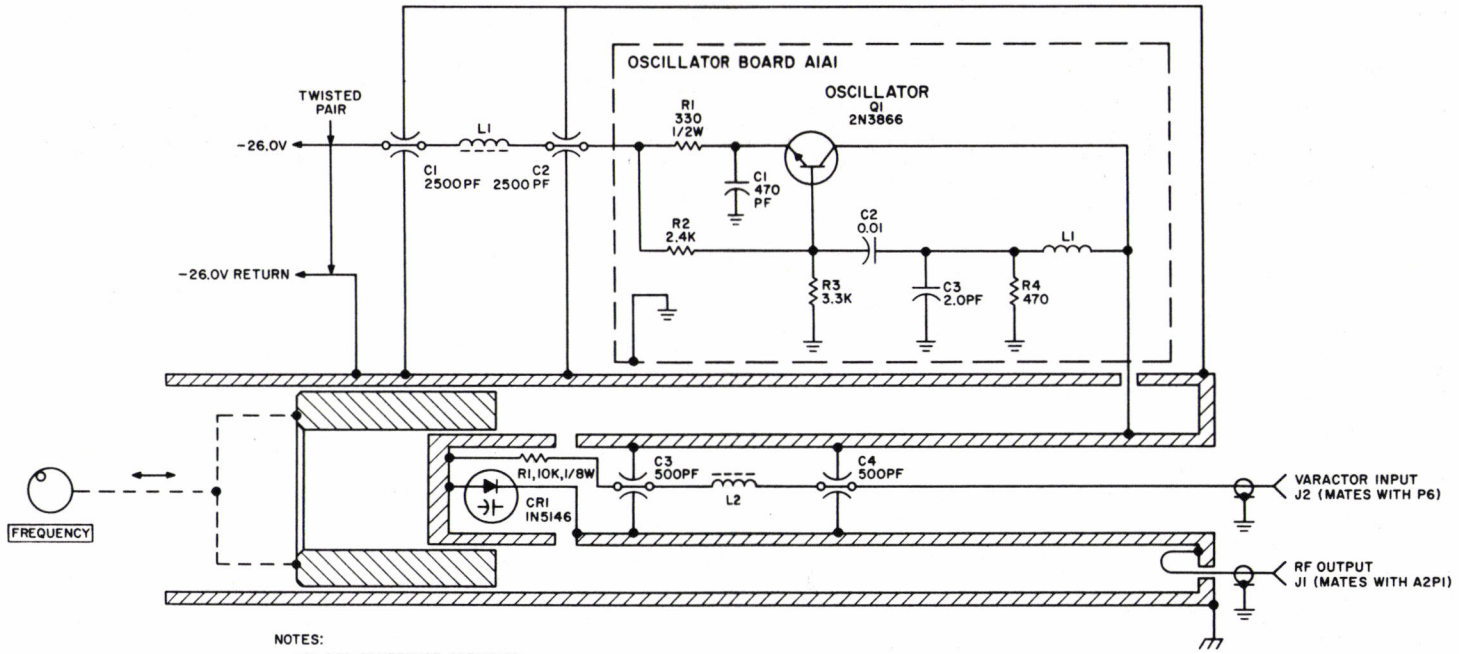
j. Couple an H-P 651B test oscillator to the FM connector. Tu the test oscillator to 41.58 kHz (using an Eldorado 1650 counter) and adjust its output level for the first carrier null on the spectrum analyzer.

k. Adjust FM dev mtr cal potentiometer A7R77 for a full-scale reading (100 kHz) on the % AM/FM DEV meter.

4-163. CALIBRATING POWER SUPPLIES AND COUNTER.

4-164. To calibrate Power Supply, see Table 4-2.

4-165. To calibrate Counter, see paragraph 4-42.




NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
2. ALL CAPACITOR VALUES ARE IN MICROFARADS

Figure 6-2. Master Oscillator A1, Schematic Diagram.

MODEL 6201

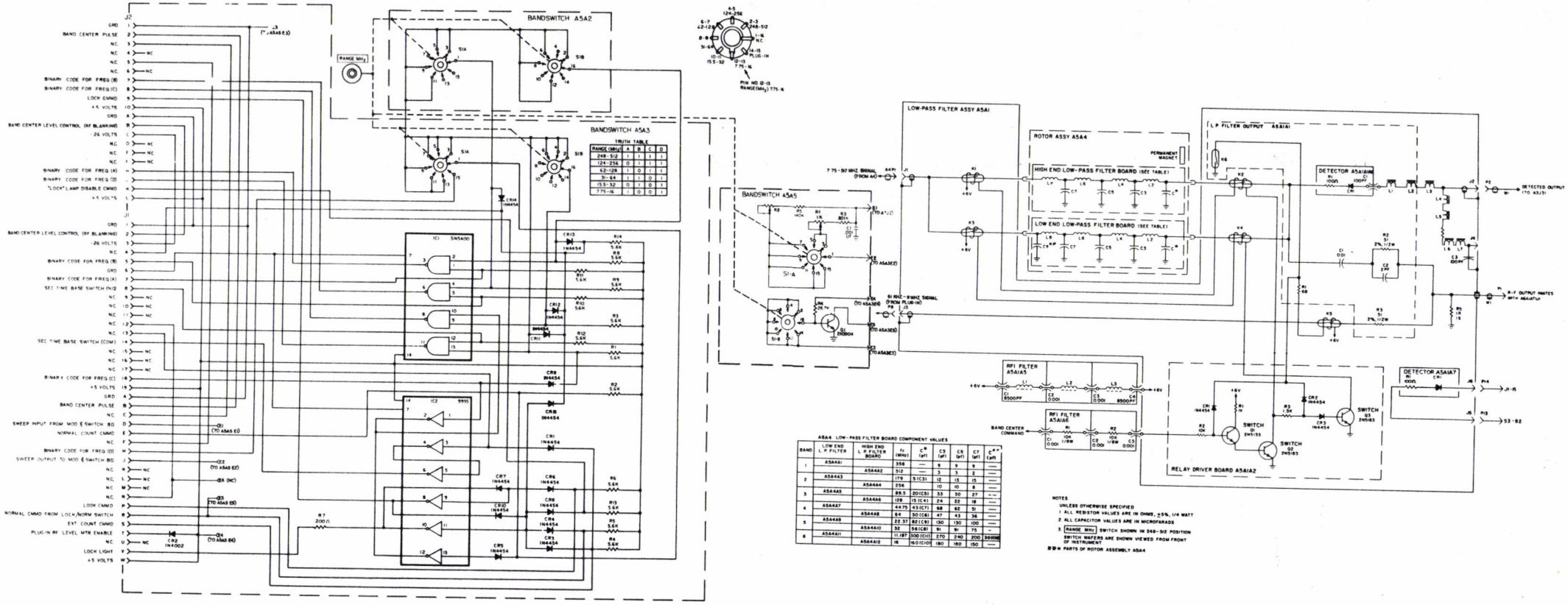
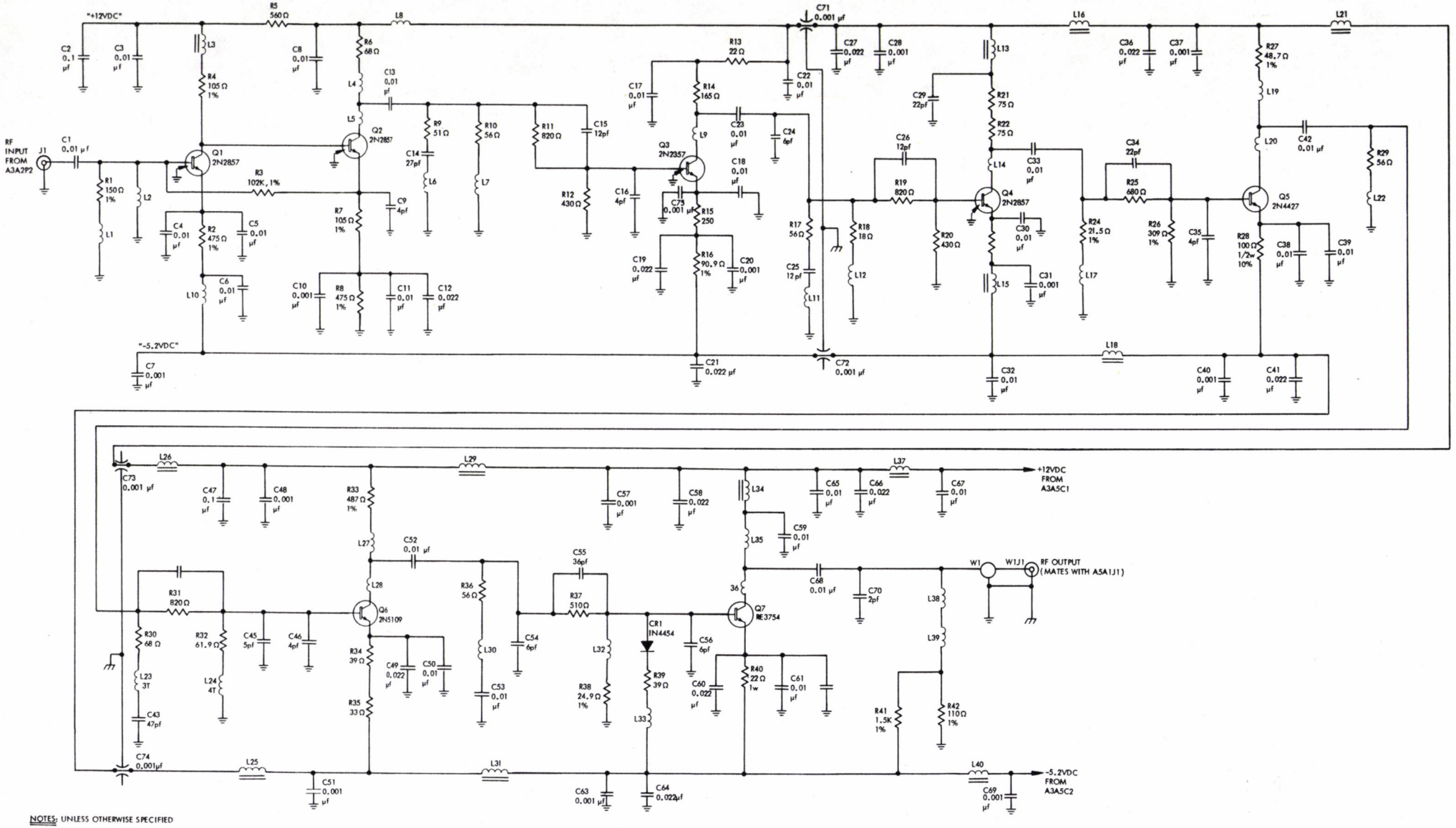



Figure 6-15. Low Pass Filter A5, Schematic Diagram.




NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS 1/4w, 5%.

Figure 6-5. Power Amplifier, 5Ω, 520 MHz, A4A1, Schematic Diagram.

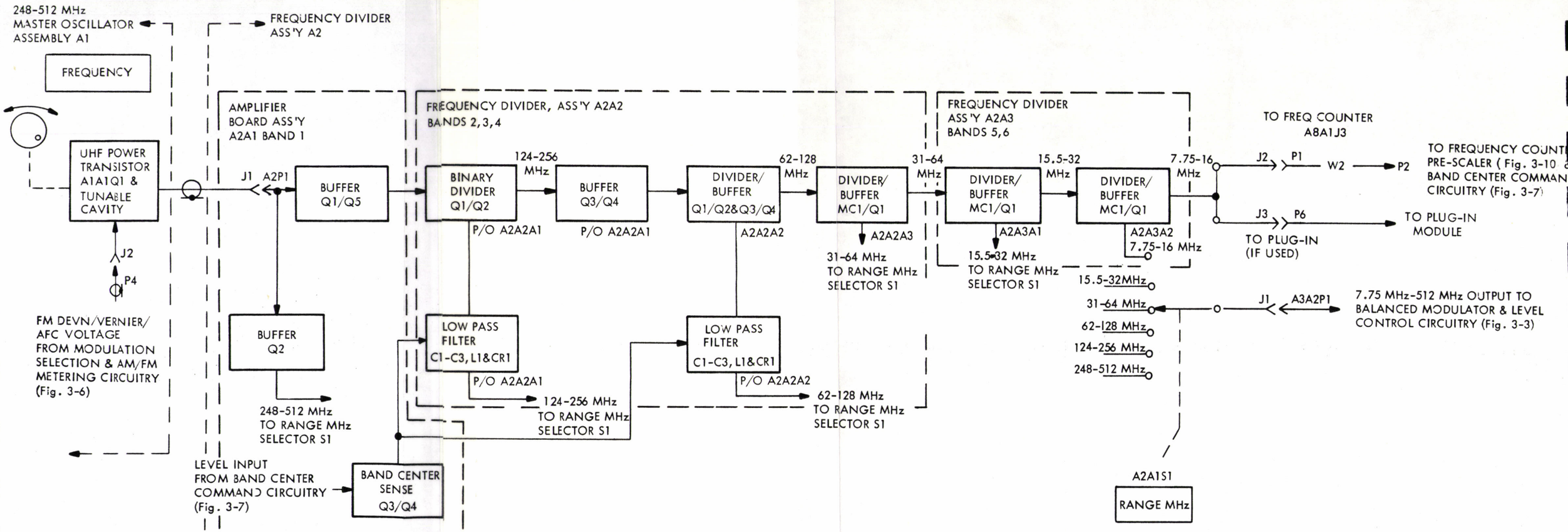



Figure 3-2. Frequency Generation Circuitry, Detailed Block Diagram

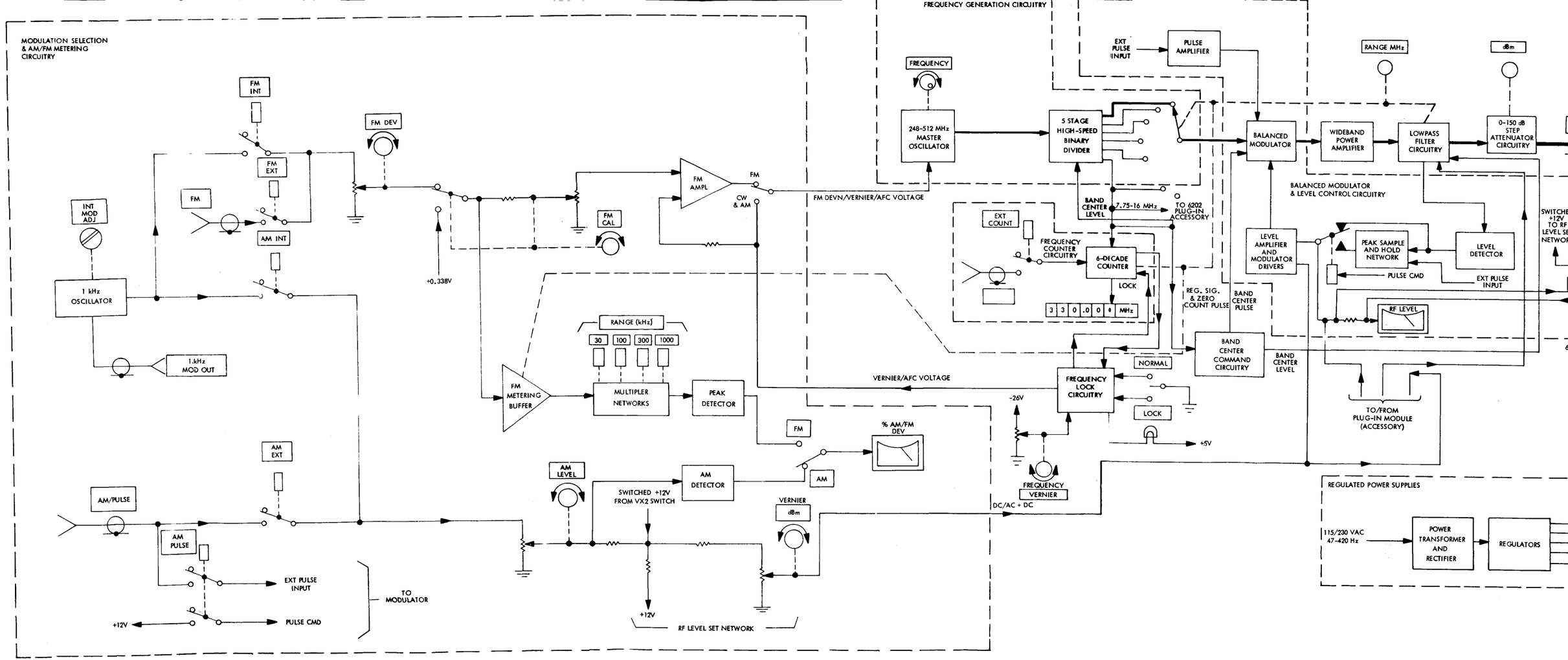
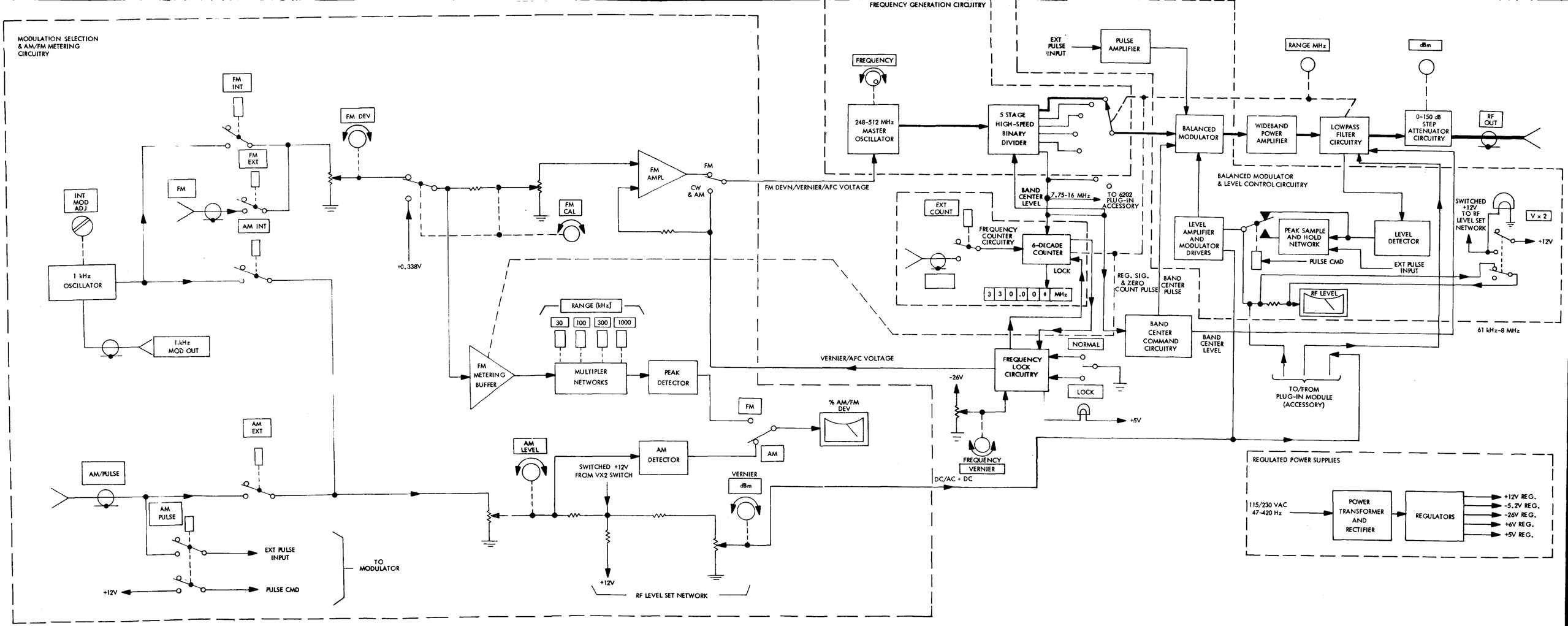
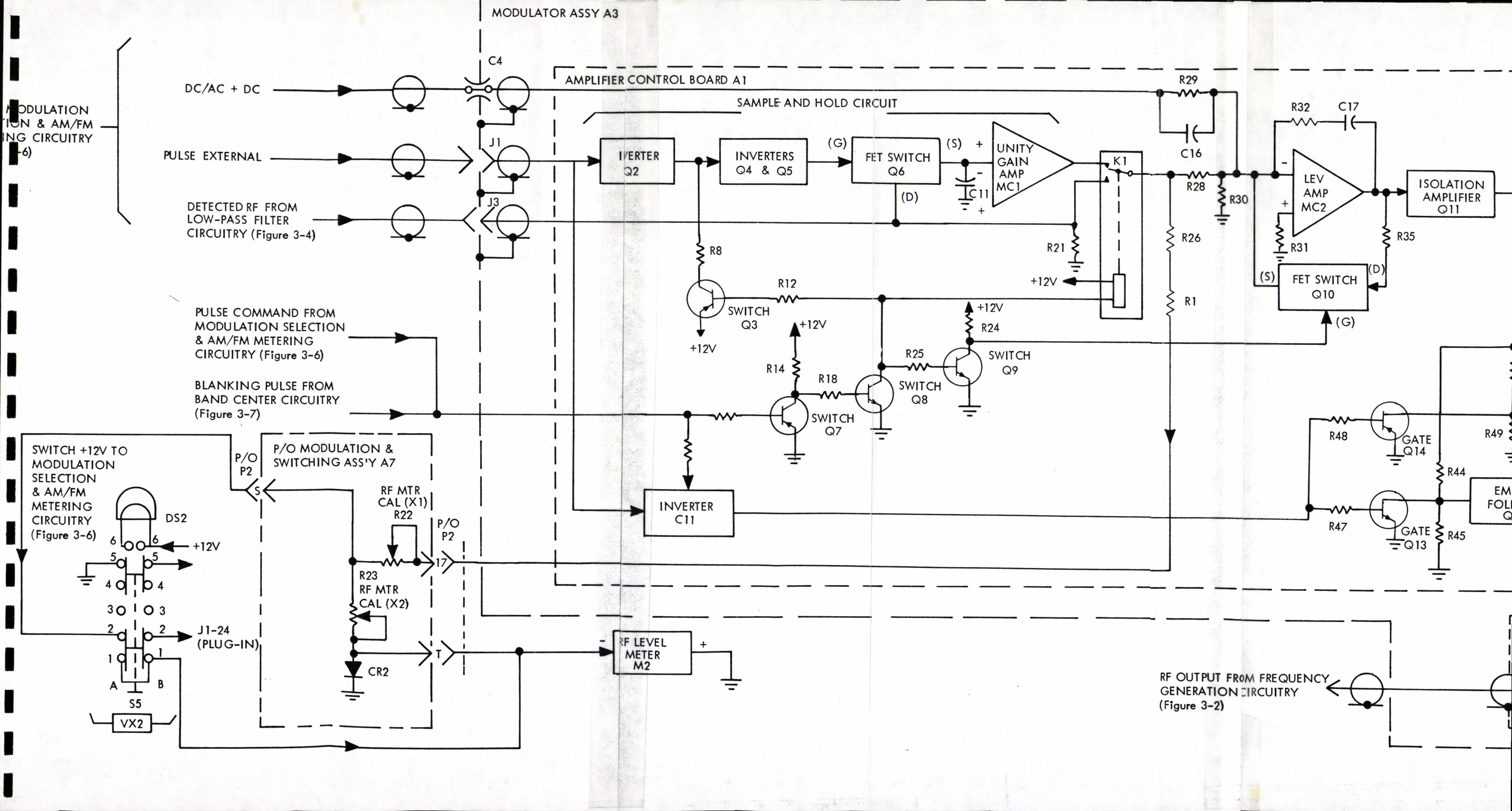



Figure 3-1. 6201 Signal Generator, Simplified Functional Diagram




3-1

Figure 3-1. 6201 Signal Generator, Simplified Functional Diagram


MODULATOR ASSY A3
AMPLIFIER CONTROL BOARD A1
SAMPLE AND HOLD CIRCUIT
DC/AC + DC
PULSE EXTERNAL
DETECTED RF FROM LOW-PASS FILTER CIRCUITRY (Figure 3-4)
C4
J1
J3
INVERTER Q2
INVERTERS Q4 & Q5
FET SWITCH Q6
UNITY GAIN AMP MC1
C11
K1
R29
C16
R32
C17
R28
R30
LEV AMP MC2
R31
ISOLATION AMPLIFIER Q11
R35
R26
R1
R21
+12V
R8
R12
SWITCH Q3
FET SWITCH Q10
(S)
(D)
(G)
PULSE COMMAND FROM MODULATION SELECTION & AM/FM METERING CIRCUITRY (Figure 3-6)
BLANKING PULSE FROM BAND CENTER CIRCUITRY (Figure 3-7)
R14
R18
R25
R24
SWITCH Q7
SWITCH Q8
SWITCH Q9
INVERTER C11
R48
GATE Q14
R49
R44
R47
GATE Q13
R45
SWITCH +12V TO MODULATION SELECTION & AM/FM METERING CIRCUITRY (Figure 3-6)
P/O P2
P/O MODULATION & SWITCHING ASS'Y A7
DS2
RF MTR CAL (X1) R22
R23 RF MTR CAL (X2)
CR2
J1-24 (PLUG-IN)
S5
VX2
RF LEVEL METER M2
RF OUTPUT FROM FREQUENCY GENERATION CIRCUITRY (Figure 3-2)

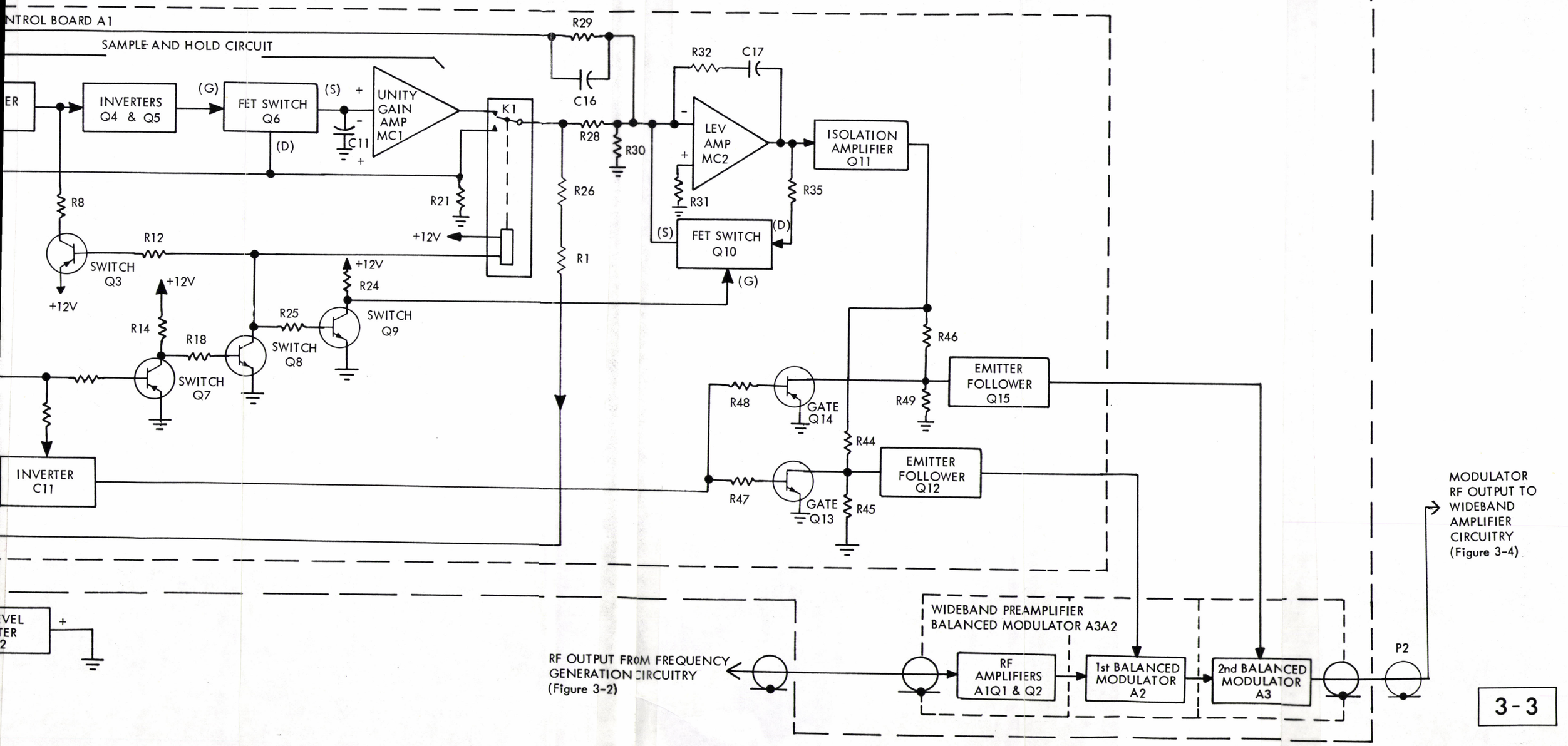
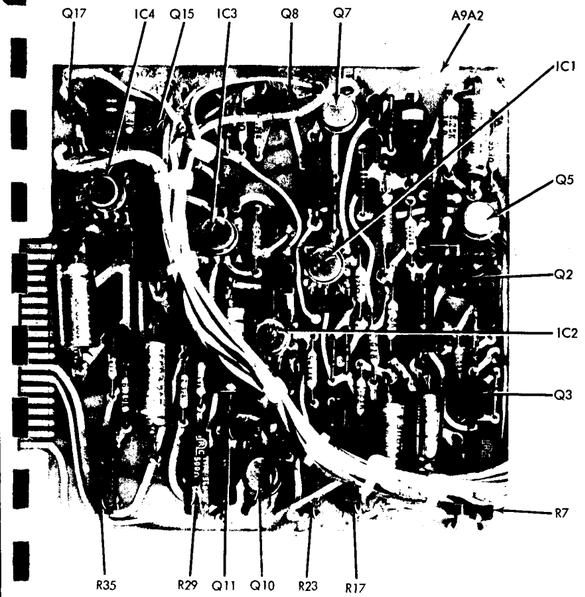
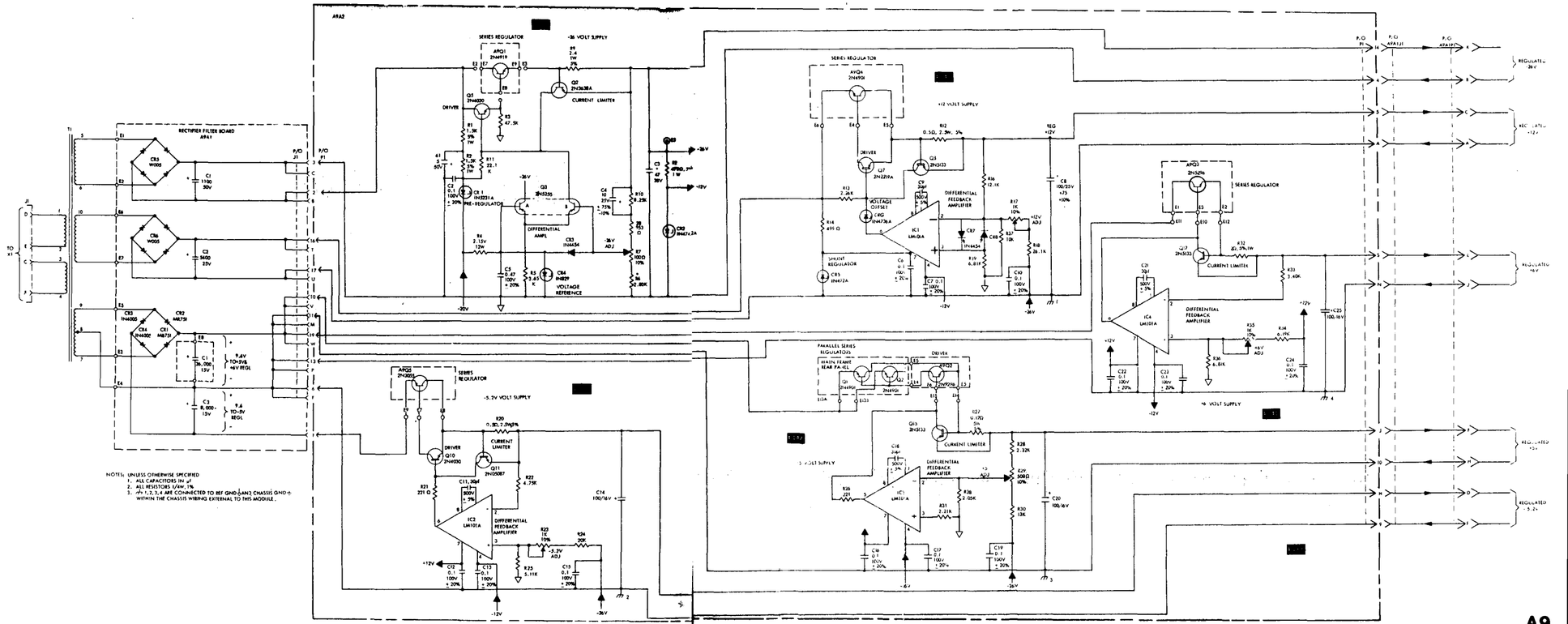



Figure 3-3. Balanced Modulator and Level Control Circuitry, Detailed Block Diagram

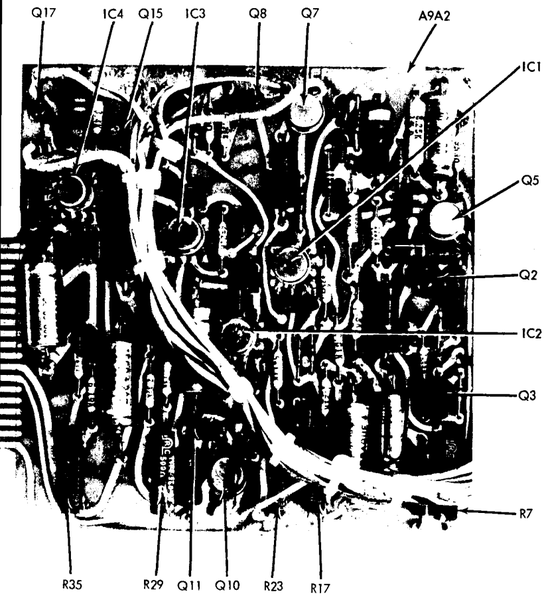


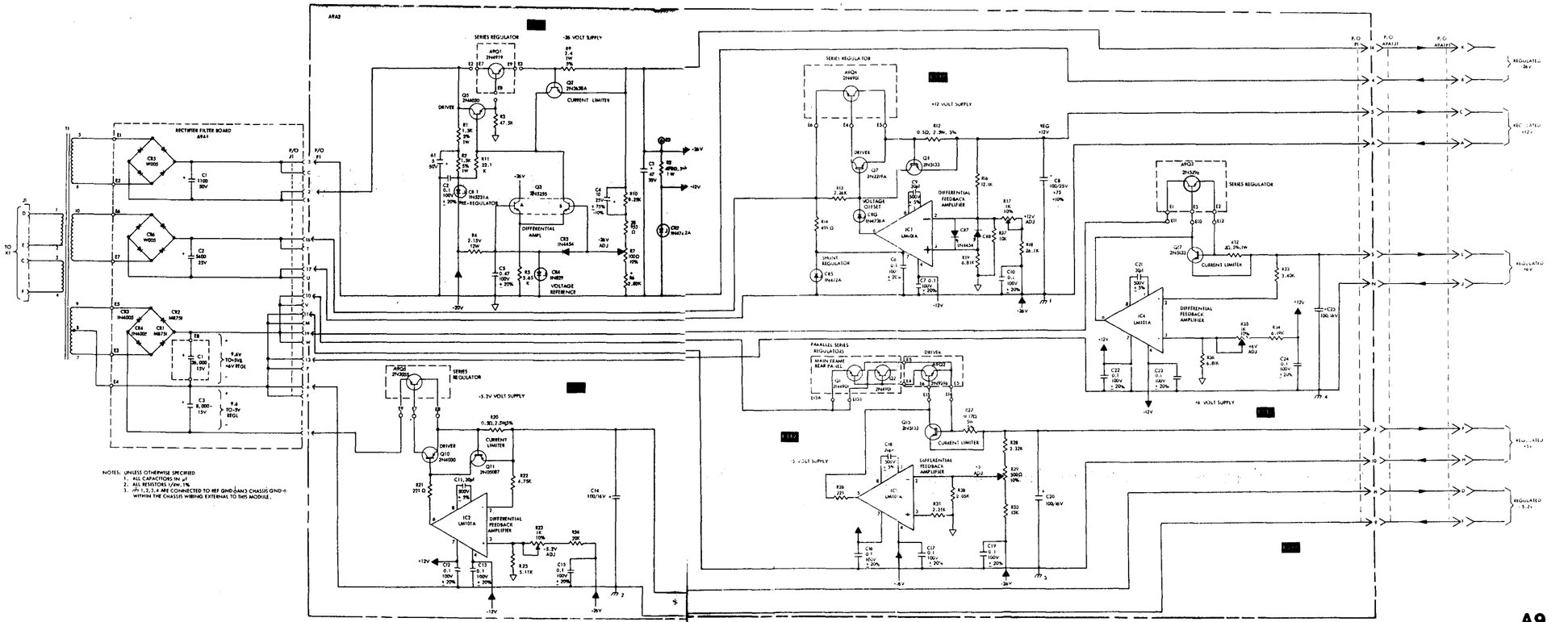




A9

4 -33.

Figure 4-33. Regulated Power Supplies, Functional Schematic Diagram

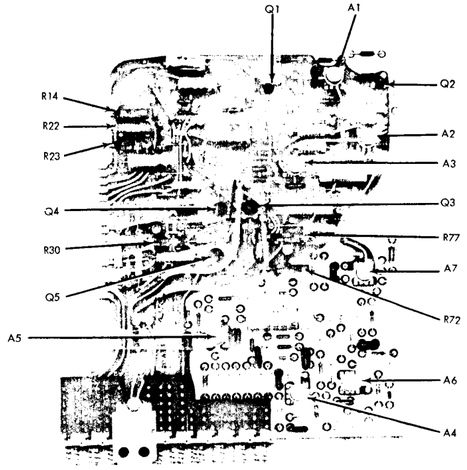



A9

4-33.

Figure 4-33. Regulated Power Supplies, Functional Schematic Diagram




**A7**
Parts Locations

MODULATION & SWITCHING ASSEMBLY A7

AFC VERNIER VOLTAGE FROM FREQUENCY LOCK CIRCUITRY (FIGURE 4-32)

P/O P2

FM J17

C41 2.2 35V

-5.2V

1 kHz OSCILLATOR

SWITCHED +12V

CR3 1N4148

CR5 1N4148

R37 10K

R36 464

CR4 1N4148

R35 866

R38 10K

R25 1K

C7 33 25V

R31 4.75K

C6 120 pF 500V ±2%

R30 100K

C8 50V ±20%

R32 806

A1 LM101A

R28 100K

R29 100K

Q2 2N5460

R26 1K

C9 .01 200V

R34 14.7K

C10 .01 200V

R33 13.7K

C11 120 pF 500V ±2%

A2 LM101A

R88 1.00K

-26V

C12 .1 200V ±2%

R39 15.8K

C13 200V ±2%

R40 162

R41 162

A3 LM101A

C14 120 pF 500V ±2%

R42 100

R43 100

R44 1K

C17 2.2 100V

CR12 1N4742A

C15 2.2 100V

C16 2.2 100V

E1 E2 E3 E4 E5 E6

R45 100

TP3

FM CAL VOLTS ADJ

R79 49.9

R80 500 ±10%

R81 1.5K

+12V

RANGE MHz

P/O BANDSWITCH A5A5

P/O A5A3J1

P/O P1

R4 78K

R2 14K

R1 3.4K

R11 2.6

R3 7K

R6 59K

R5 3.01K

R8 51.1K 78K

R7 9

R10 127K

R13 76.7K

FM CAL R5 1K

R6 1K ±1% 1 kW

P/O P2

S4 CW

S5 FM INT

S6 FM EXT

DS1 +12V

TO S3

P/O P2

FM DEV VERNIER/AFC VOLTAGE TO FREQUENCY GENERATION CIRCUITRY (FIGURE 4-15)

FM DEV R2 1K

P/O S3 (FM CAL)

R52 15.0

R54 15.0

R53 750 1/2W

P/O P2

MOD OUT 1 kHz J11

P/O P2

EXT PULSE INPUT

PULSE CMD (SWITCHED +12V)

R1 1K

AM LEVEL

TO BALANCED MODULATOR & LEVEL CONTROL CIRCUITRY (FIGURE 4-16)

SWITCHED +12V FROM VX2 PUL FROM VX3 PUSHBUTTON (FIGURE 4-16)

P/O P2

SWITCHED +12V

P/O P2

R3 5K

-26V

-5.2V

+12V

GND

AM PULSE J10

P/O P2

S1 AM PULSE

S2 AM EXT

S3 AM INT

FROM CW LAMP DS1

+12V

** FACTORY-SELECTED; INSTALLED TEST
* FACTORY-SELECTED; NOMINAL VALUE SHOWN
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 1%
1. ALL CAPACITOR VALUES ARE IN MICROFARADS

NOTES, UNLESS OTHERWISE SPECIFIED:

+12V

4.78

C150 15 +75% -10%

MAX LEV SET (X1)

R3* 1.40K

MAX LEV SET (X2)

R5 619

C3 10 15V +75% -10%

R6 1.87K

ZERO BAL

*R4 392

C2 50 15V +75% -10%

-5.2V

+12V

4.84

R7 33.2K

R8 18.2K

R9 562

C4 35 15V +75% -10%

Q1 2N5133

R10 365

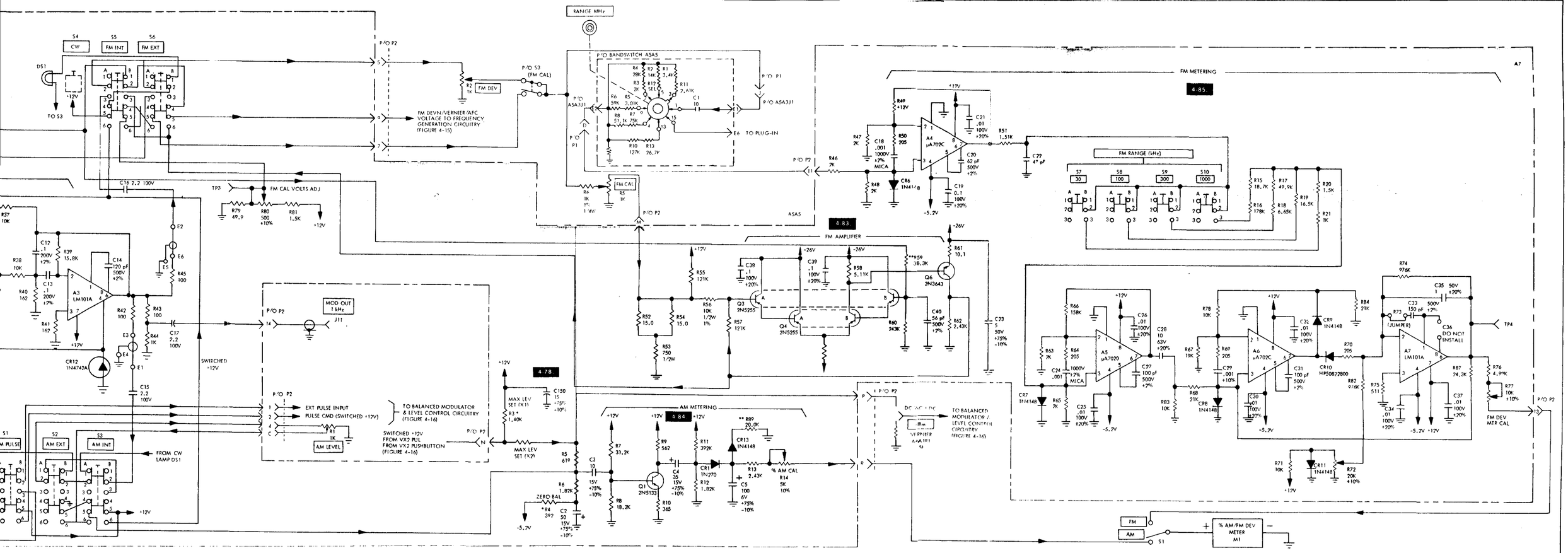
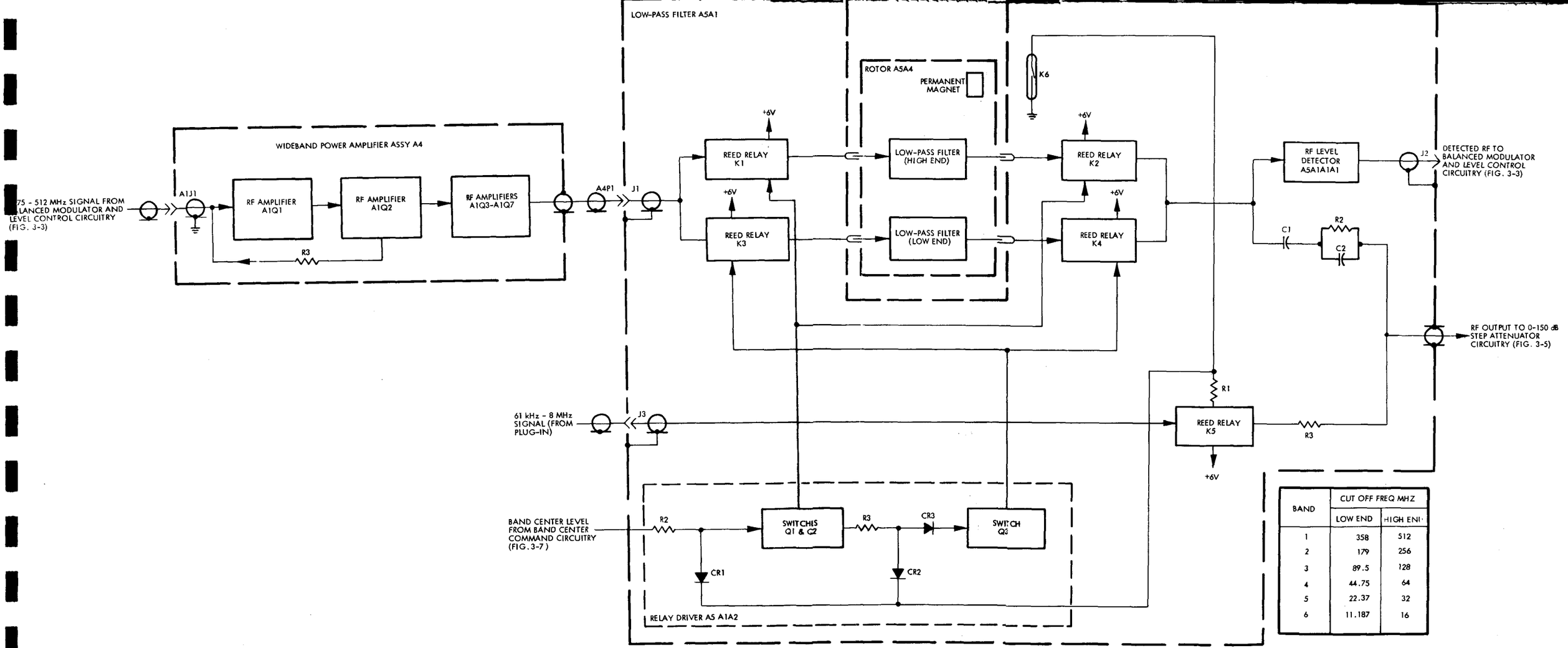



Figure 4-20. Modulation Selection and AM/FM Metering Circuitry

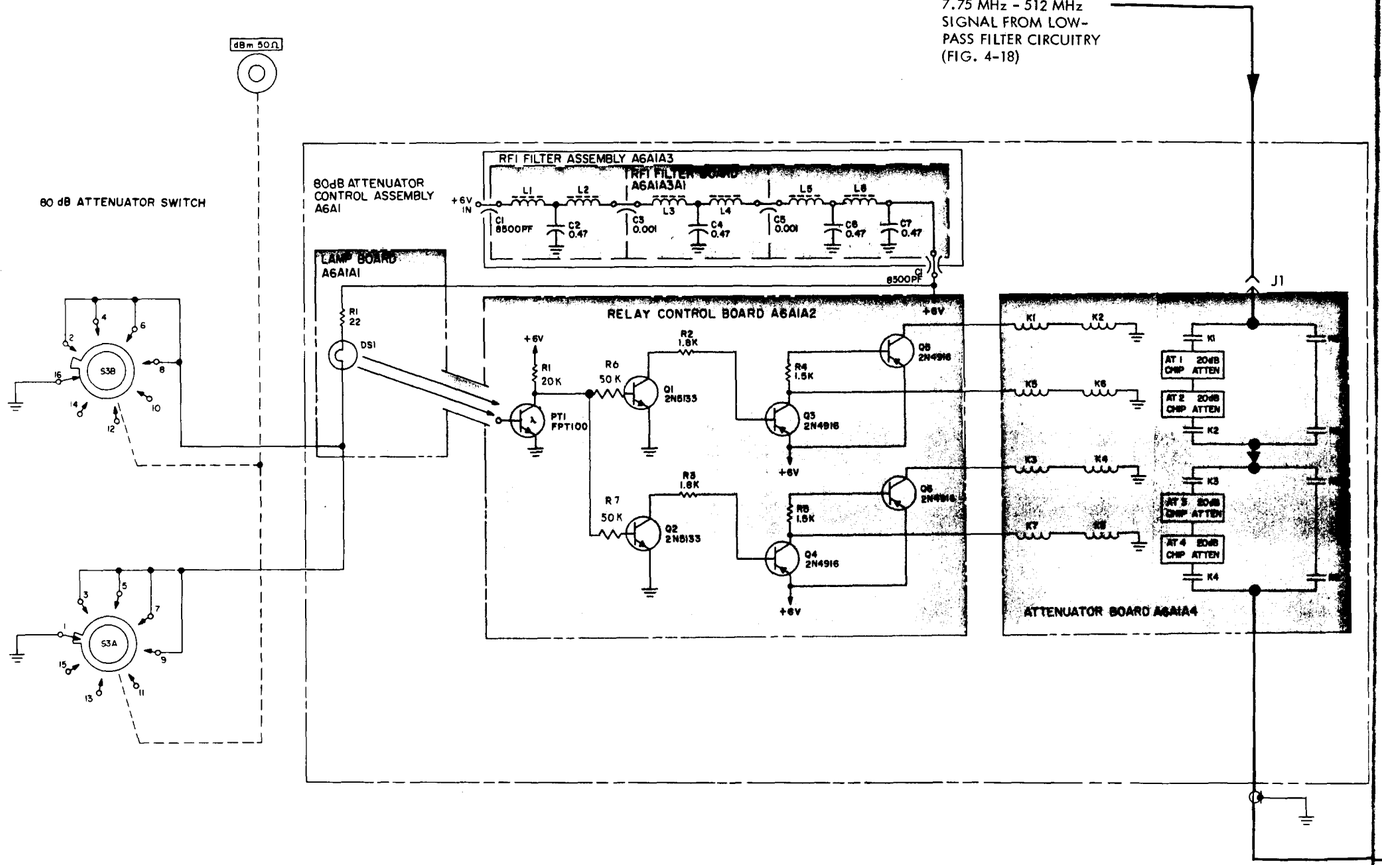


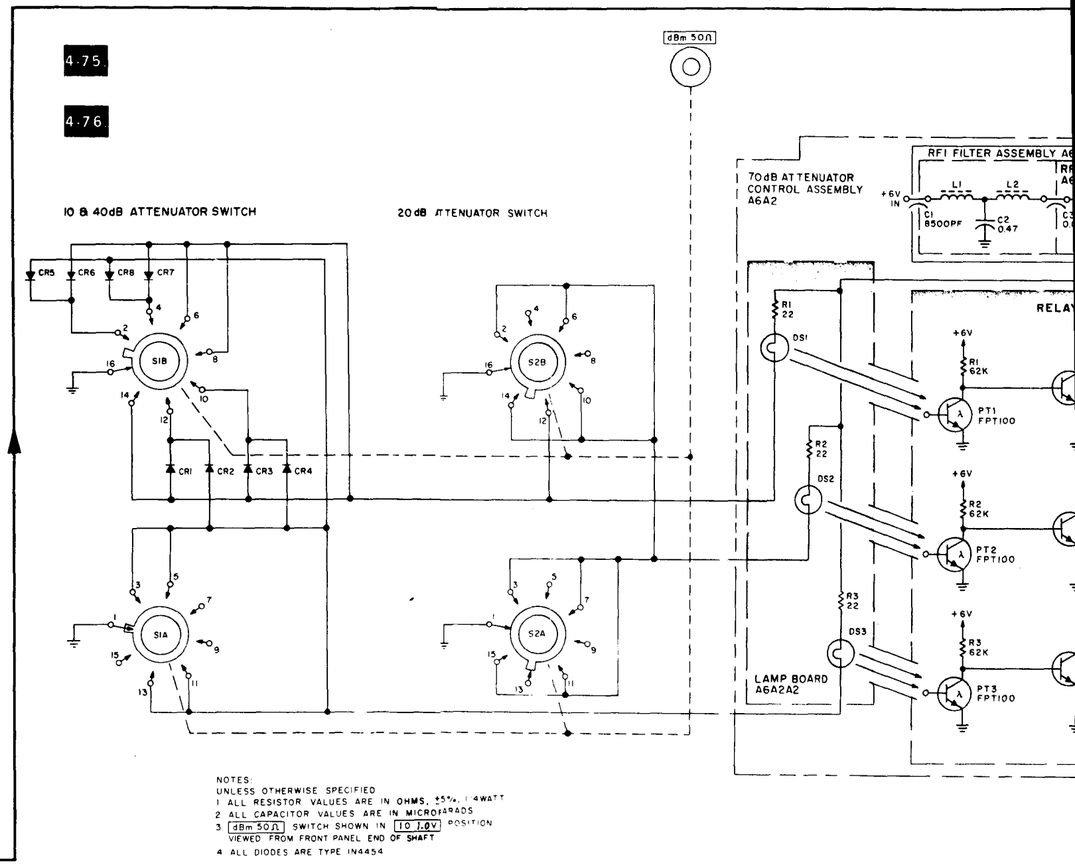

| BAND | CUT OFF FREQ MHZ | |
|---|---|---|
| | LOW END | HIGH END |
| 1 | 358 | 512 |
| 2 | 179 | 256 |
| 3 | 89.5 | 128 |
| 4 | 44.75 | 64 |
| 5 | 22.37 | 32 |
| 6 | 11.187 | 16 |

FIGURE 3-4. WIDEBAND POWER AMPLIFIER AND LOW-PASS FILTER CIRCUITRY, DETAILED BLOCK DIAGRAM



Figure 3-4. Wideband Power Amplifier and Low-Pass Circuitry, Detailed Block Diagram



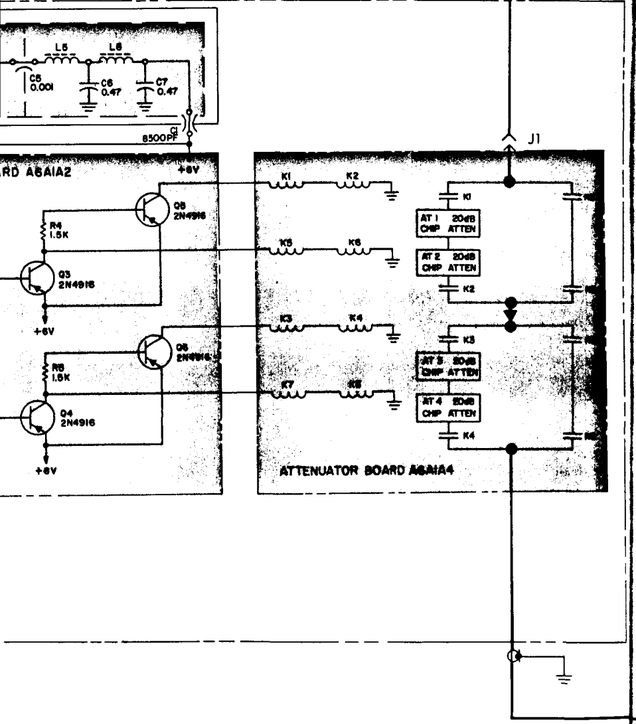



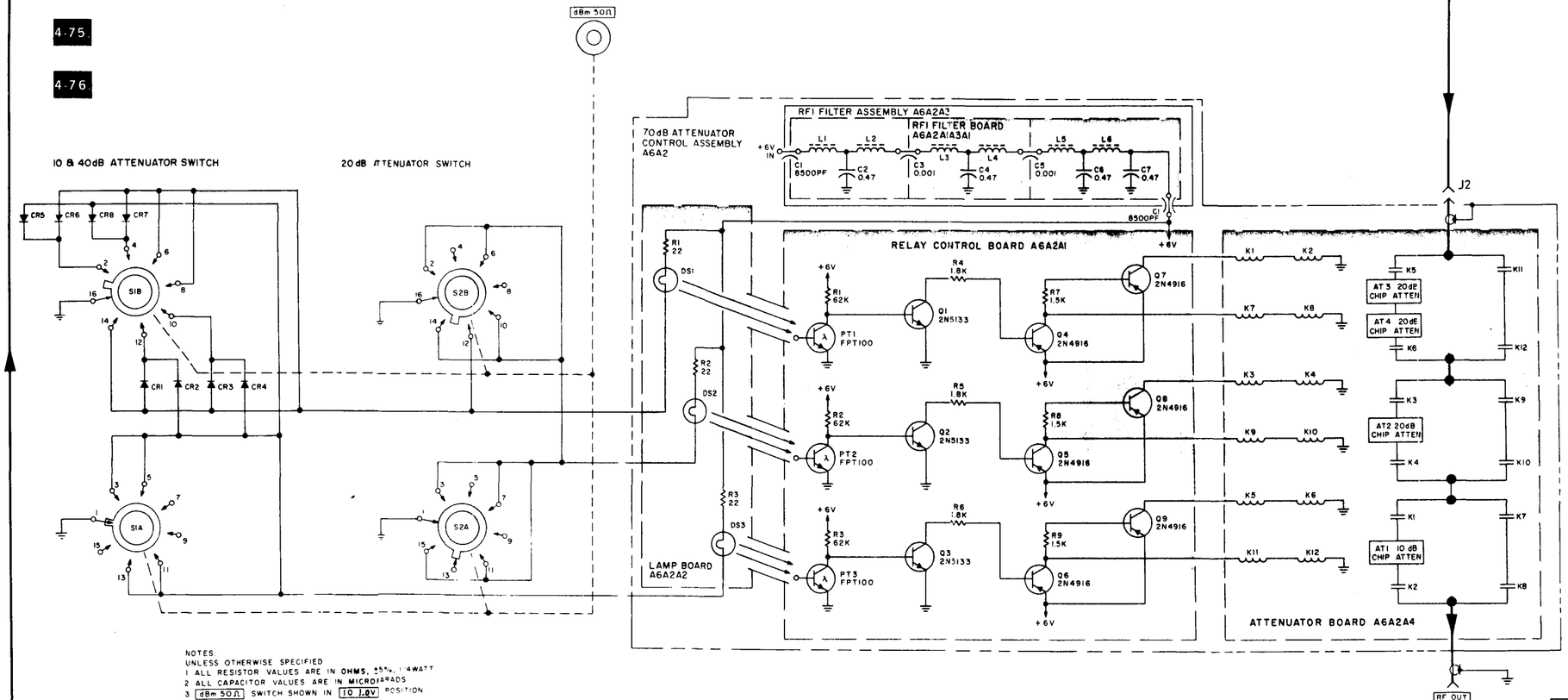

NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4WATT
2 ALL CAPACITOR VALUES ARE IN MICROFARADS
3 dBm 50Ω SWITCH SHOWN IN 10 1.8V POSITION
VIEWED FROM FRONT PANEL END OF SHAFT
4 ALL DIODES ARE TYPE IN4454

7.75 MHz - 512 MHz SIGNAL FROM LOW-PASS FILTER CIRCUITRY (FIG. 4-18)

4-75

4-76



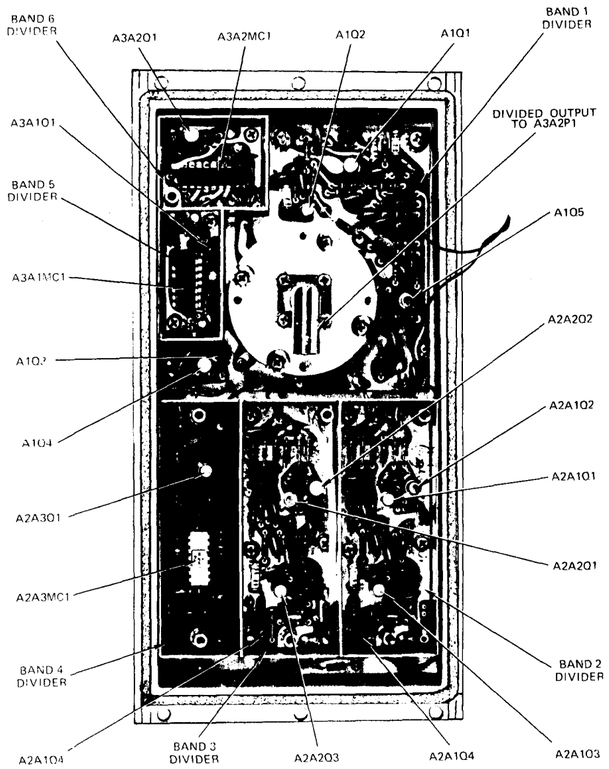




NOTES:
UNLESS OTHERWISE SPECIFIED
1 ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4WATT
2 ALL CAPACITOR VALUES ARE IN MICROFARADS
3 dBm 50Ω SWITCH SHOWN IN TO 1.0V POSITION VIEWED FROM FRONT PANEL END OF SHAFT
4 ALL DIODES ARE TYPE 1N4454

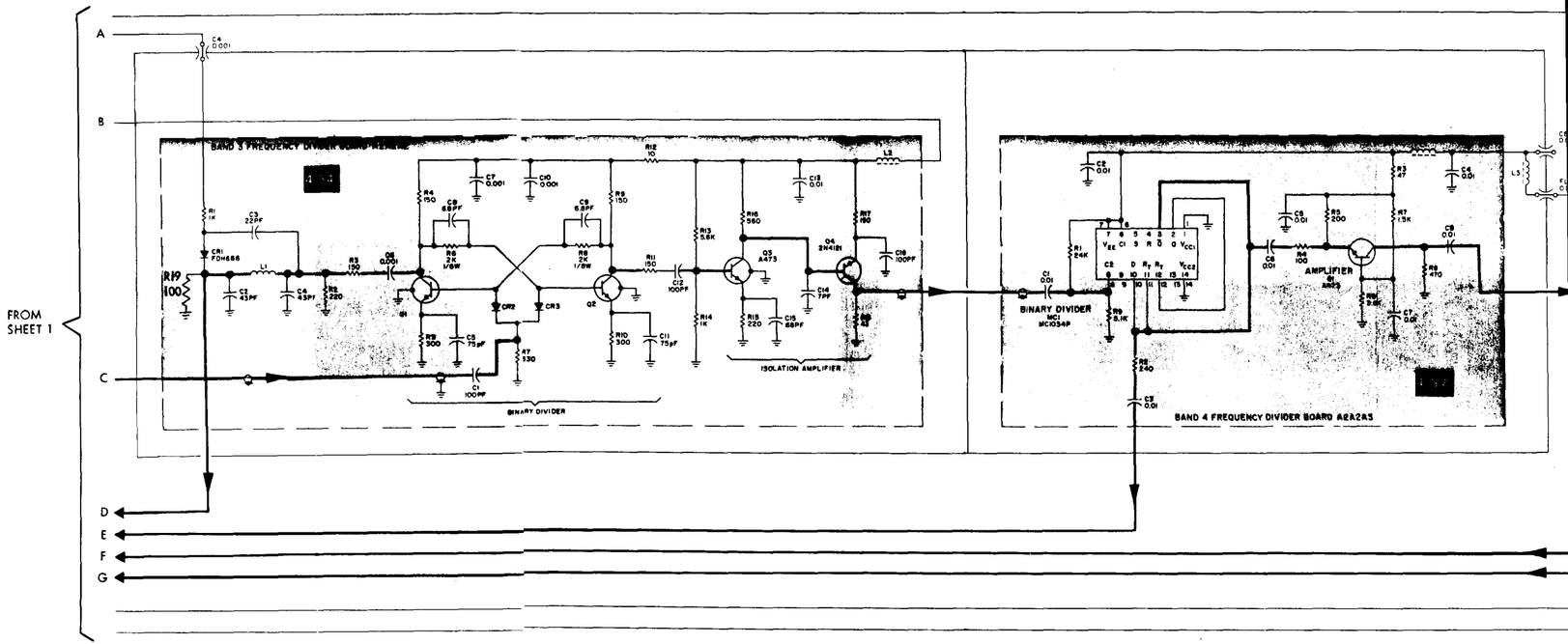
A6

4-19

Figure 4-19. 0-150 dB Step Attenuator Circuitry, Functional Schematic Diagram




**A2**
Parts Locations



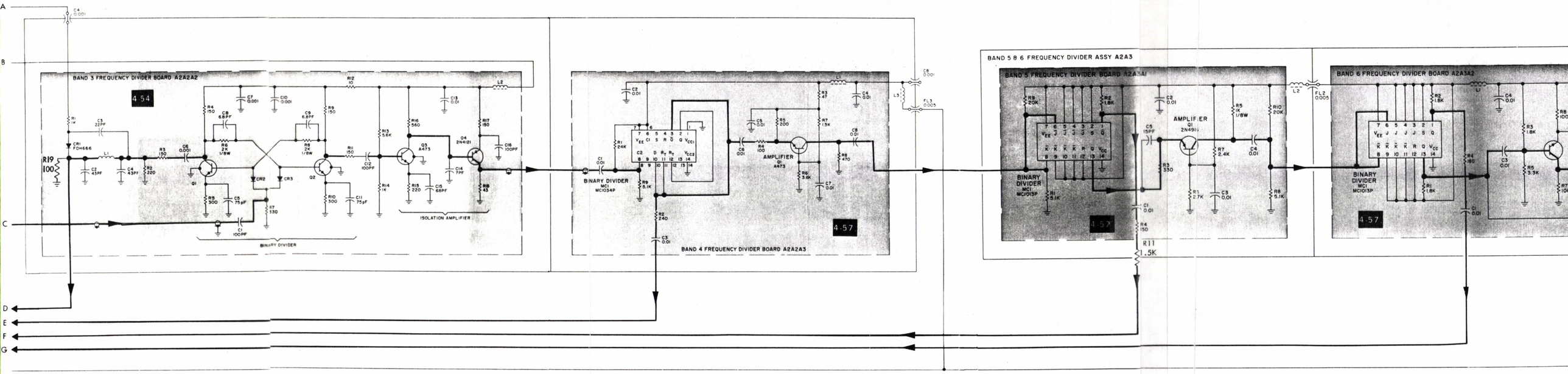
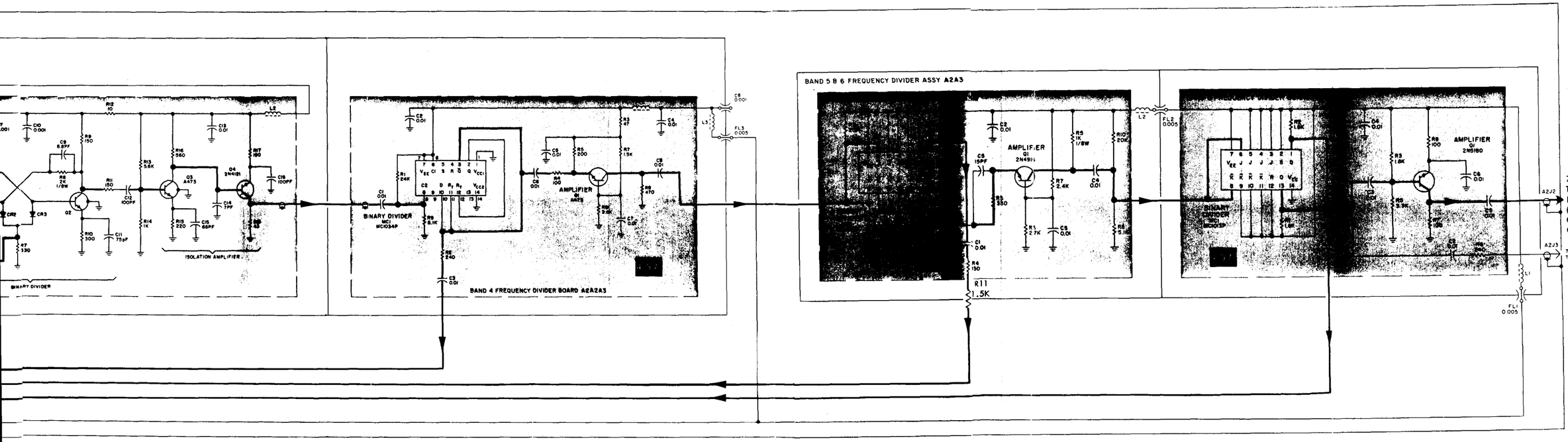


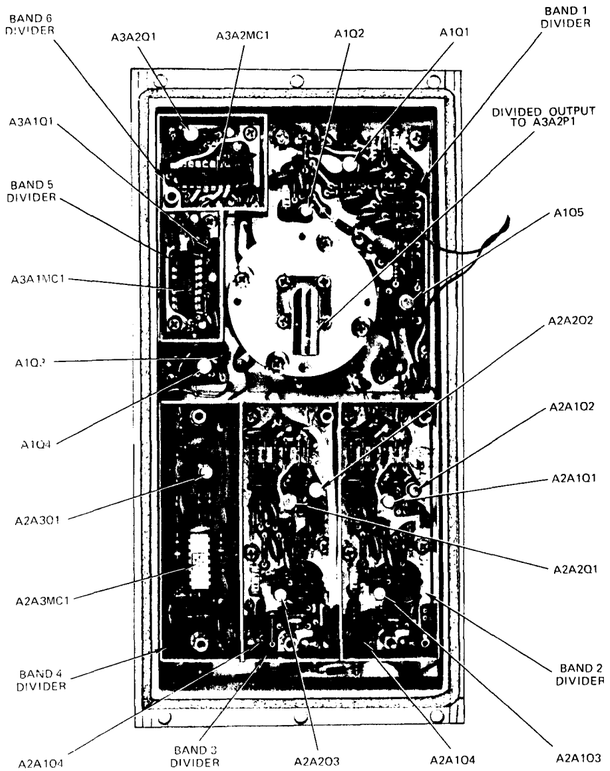

Figure 4-15. Frequency Generatio



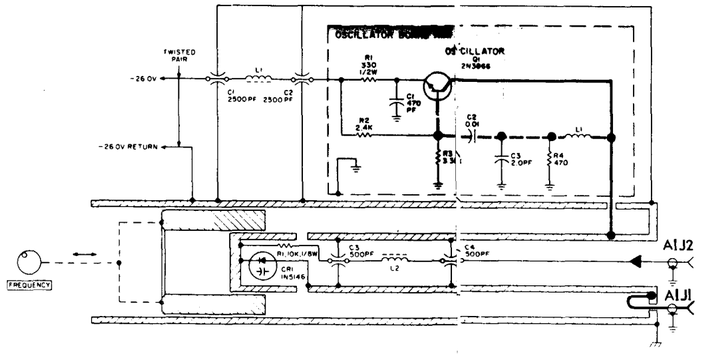

A2

4 - 15.

Figure 4-15. Frequency Generation Circuitry, Functional Schematic Diagram (Sheet 2 of 2)

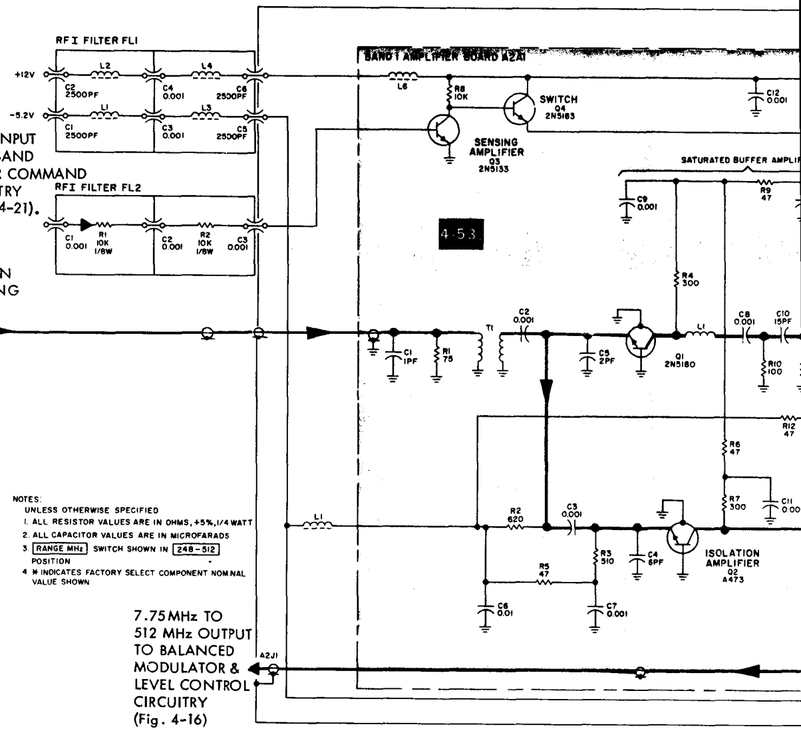



**A2**
Parts Locations




FM DEVN/VERNIER/AFC VOLTAGE FROM MODULATION SELECTION & AM/FM METERING CIRCUITRY (FIGURE 4-20).

LEVEL INPUT FROM BAND CENTER COMMAND CIRCUITRY (FIGURE 4-21).




NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. RANGE MHz SWITCH SHOWN IN 248-512 POSITION
4. M INDICATES FACTORY SELECT COMPONENT NOMINAL VALUE SHOWN

7.75 MHz TO 512 MHz OUTPUT TO BALANCED MODULATOR & LEVEL CONTROL CIRCUITRY (Fig. 4-16)

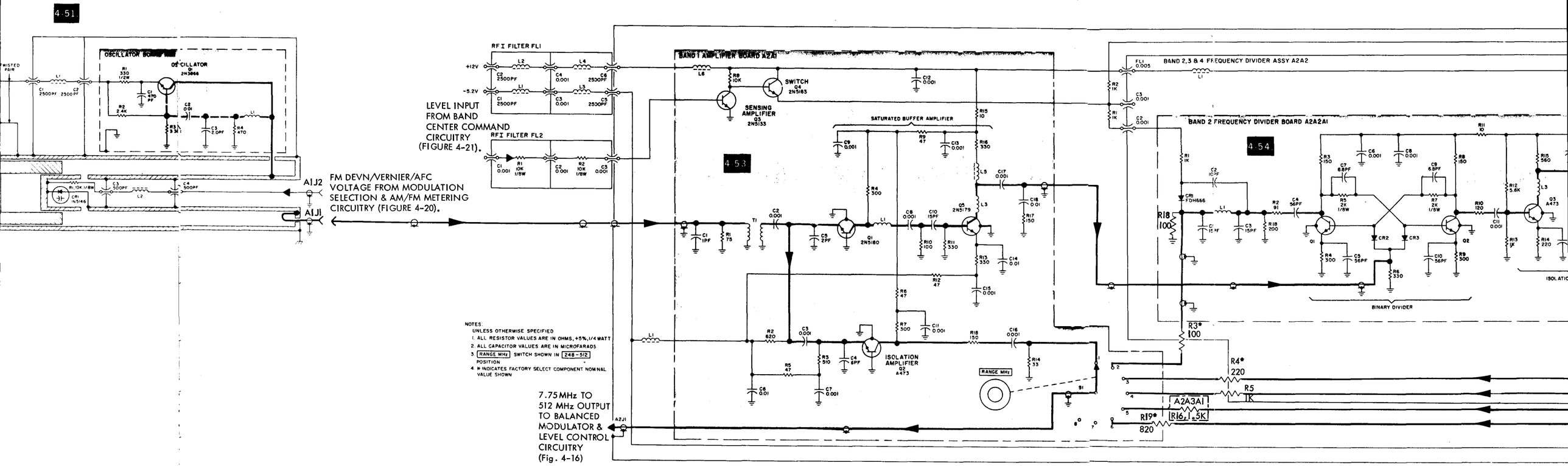
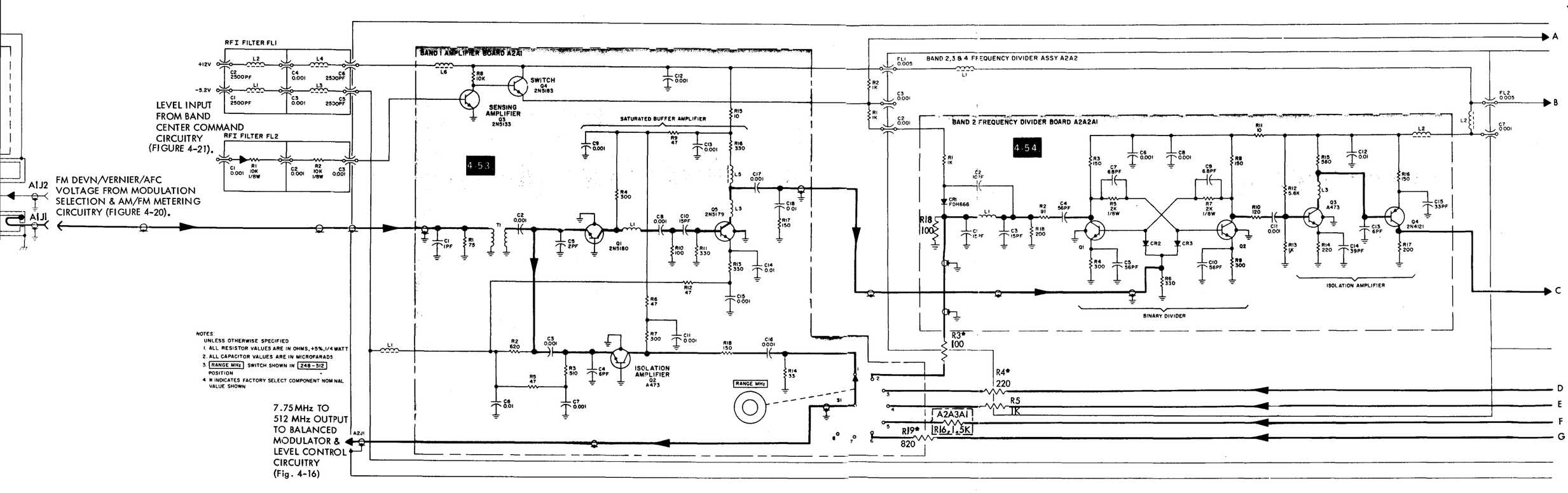



Figure 4-15. Frequency Ge

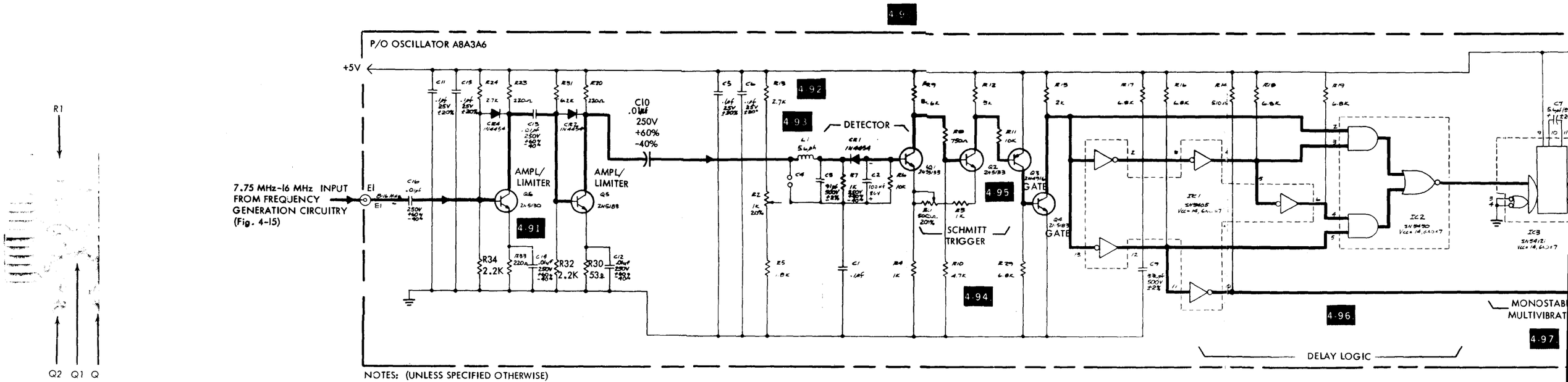



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 WATT
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. RANGE MHz SWITCH SHOWN IN 248-512 POSITION
4. * INDICATES FACTORY SELECT COMPONENT NOMINAL VALUE SHOWN

**A1/A2**

**4-15.**

Figure 4-15. Frequency Generation Circuitry, Functional Schematic Diagram (Sheet 1 of 2)

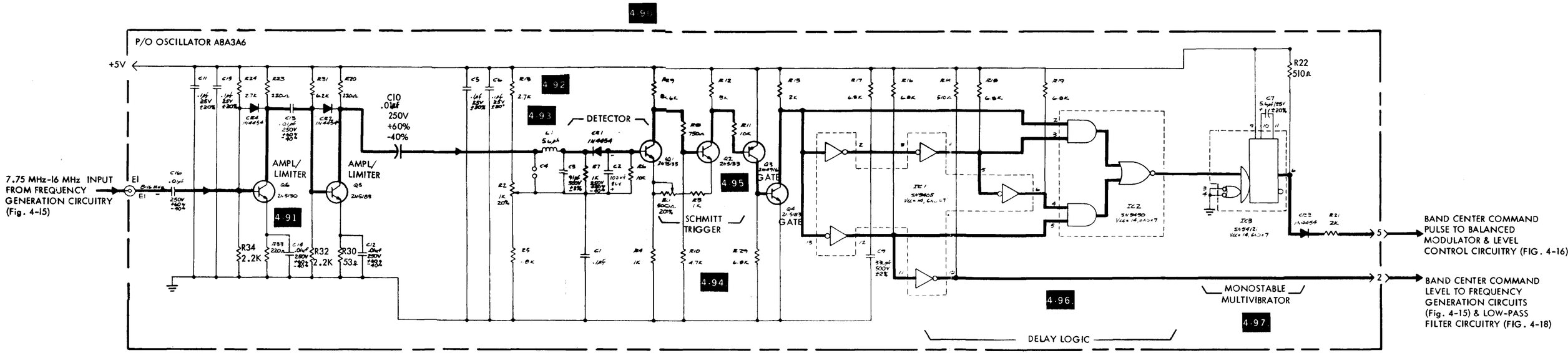



NOTES: (UNLESS SPECIFIED OTHERWISE)

1. ALL RESISTORS 1/4 W, 5% CARBON.

*FACT. SELECT, NOMINAL VALUE SHOWN

Figu




NOTES: (UNLESS SPECIFIED OTHERWISE)

1. ALL RESISTORS 1/4 W, 5% CARBON.

*FACT. SELECT, NOMINAL VALUE SHOWN

**A8/A3/A6**

**4-21.**

Figure 4-21. Band Center Command Circuitry, Functional Schematic Diagram

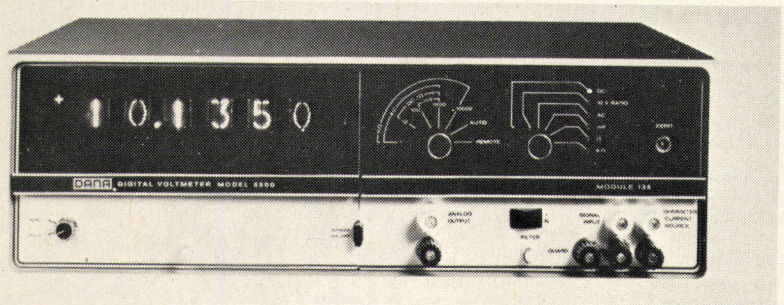
namelijk: model 15-6347-00 met papiersnelheden van 1, 5, 25 en 125 mm/s en mm/min en model 15-6347-10 met snelheden van 5, 10, 15 en 50 mm/s en mm/min.
Evenals de andere lijnschrijvers van dit fabrikaat is dit model uitgerust met het door Brush gepatenteerde inktsysteem met onder druk staande inkt, waarmee droge, veegvrije en nietvlekkende lijnen worden verkregen. De inkt bevindt zich in wegwerp-inktpatronen. Bij wegvallen van de spanning of beëindigen van de papierstrook stopt het schrijfmechanisme onmiddellijk en wordt de inkt van de penpunt weggezogen, zodat vlekken en morsen zijn uitgesloten.
Het servosysteem voor de beweging van de schrijfstift is gebaseerd op een grote nauwkeurigheid en is de kans op doorschot uitgesloten. De motor van de schrijfstift en de transductor zijn volledig afgesloten, zodat het apparaat geschikt is voor gebruik onder de meest ongunstige bedrijfsomstandigheden.
Bij 50 schaaldelen is de frequentiekarakteristiek vlak binnen 2% van de volle schaaluitslag in het gebied van gelijkstroom tot 40 Hz. Bij 10 schaaldelen is de frequentiekarakteristiek vlak binnen 2% van de volle schaaluitslag in het gebied van gelijkstroom tot 100 Hz.
Het nieuwe apparaat is geschikt voor gebruik in combinatie met de Brush-voorversterkers voor metingen in het gebied van 100 mV per schaaldeel tot 500 V volle uitslag met gekalibreerde nulpuntsonderdrukking. Tot de andere typen voorversterkers behoren normale typen en typen met zeer hoge gevoeligheid, met logaritmische of lineaire schaal, met draaggolfversterker voor gebruik met rekstrookjes, en typen voor hoge spanningen, alsmede een complete lijn van apparaten voor medische toepassingen.
De leverancier is het Laboratorium voor Elektronica N.V., Rotterdam.
(2329)

*) **Zie antwoordkaart achterin**

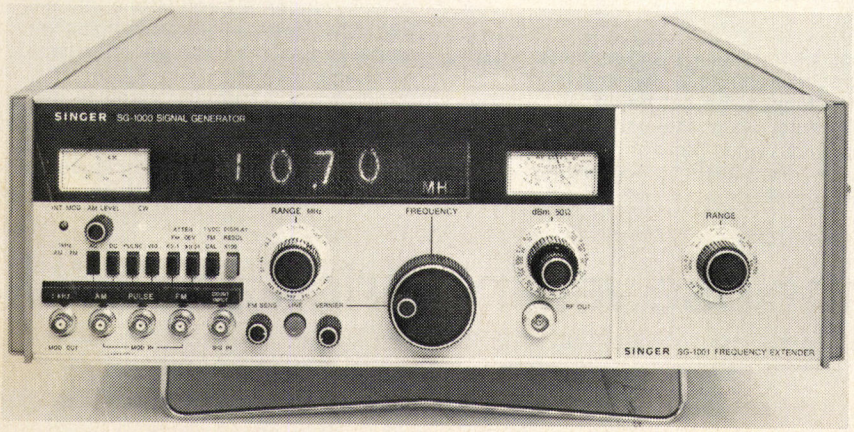
### F* Digitale multimeter

*Bijzonder geschikt voor nauwkeurig meten van effectieve waarden van diverse golfvormen*

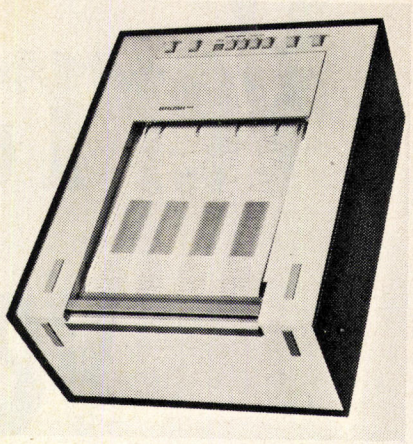
De digitale multimeter model 5500/135 van Dana Laboratories is geschikt voor het meten van:
*Gelijkspanningen,* in vijf meetgebieden vanaf 110 mV tot 1 100 V volle schaal bij een meetonnauwkeurigheid van ± 0,005 à 0,01%
*Wisselspanningen,* in vier meetgebieden van 1,1 tot 1 100 V volle schaal en frequenties van 50 Hz tot 100 kHz, bij een meetfout van ± 0,5 à 2%, afhankelijk van de golfstroom.
*Weerstandsmetingen,* in zeven meetgebieden van 11 ohm tot 11 Mohm volle schaal met een meetonnauwkeurigheid van ca. ± 1%.
*Verhoudingsmetingen* in drie meetgebieden van 1 : 1 tot 110 : 1 met eveneens een meetfout van ca. 1%.




*Digitale multimeter (Dana Laboratories)*




*Signaalgenerator SG 1000 (Singer Co.)*



*Vierkanaalsrecorder model 440 (Brush Instruments Division of Gould Inc.)*

De insteltijd varieert, afhankelijk van de ingestelde meetfunctie, van 450 tot 800 ms. Het meetresultaat kan worden afgelezen op vijf cijfereenheden en een zesde eenheid voor een overlapping van 10%. Voor zowel sinusvormige als driehoeks-, blok- en zaagtandspanningen gelden genoemde onnauwkeurigheden. De onderdrukking van gelijkfasige stoorspanningssignalen bedraagt > 140 dB. Het instrument heeft een ingebouwd vijfpoolfilter, vier aansluitklemmen voor het meten van weerstanden en een analoge uitgang. De ingangsweerstand bedraagt voor het meetgebied van 10 V:10 kohm.
De leverancier is Heijnen N.V., Gennep.
(2330)

### G* Signaalgenerator

*Zeer groot frequentiegebied (61 kHz-1 024 MHz)*

De signaalgenerator SG 1000 van Singer Co Electronic Products Division heeft een frequentiegebied van 7,75 tot 512 MHz, dat met behulp van twee inschuifeenheden naar beide zijden kan worden uitgebreid tot een totaalgebied van 61 kHz — 1 024 MHz. De ingestelde frequentie kan op vijf cijfereenheden worden afgelezen met een afleesfout van maximaal ± 0,001%. De modulatiemogelijkheden zijn talrijk: AM-modulatie van 0-20 kHz; geijkte FM-zwaai tot ± 0,5%; stijgtijdimpulsen met uitzonderlijk hoge aan/uitverhoudingen, waarbij het niveau van de amplitude van de piek automatisch wordt begrensd; lineaire breedbandige videomodulatie. Het niveau van het uitgangssignaal is nauwkeurig instelbaar tussen +20 en —146 dBm.
Toepassingsgebieden zijn: metingen aan FM-, AM- en TV-ontvangers; metingen aan en afregelen van FM-, AM- en radarzenders en vele andere metingen in het telecommunicatiegebied.
De leverancier is: Groenpol Industriële Verkoop N.V., Amsterdam.
(2331)