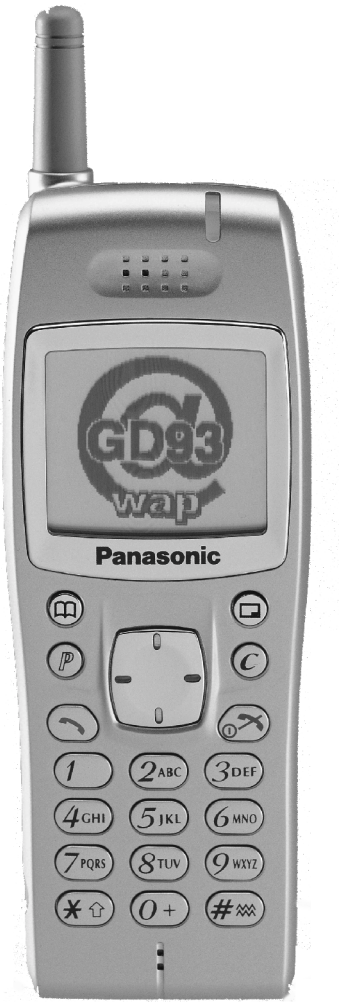
Order Number: MCUK001001G8

Technical Guide

Personal Cellular Telephone

EB-GD93

GSM



Specification

	900 MHz	1800 MHz
Frequency Range	Tx: 890 - 915MHz Rx: 935 - 960 MHz	Tx: 1710 - 1785 MHz Rx: 1805 - 1880 MHz
Tx/Rx frequency separation	45 MHz	95 MHz
RF Channel Bandwidth	200 kHz	
Number of RF channels	124	374
Speech coding	Full rate/Half rate/Enhanced Full rate	
Operating temperature	-10 °C to +55 °C	
Type	Class 4 Handheld	Class 1 Handheld
RF Output Power	2 W maximum	1 W maximum
Modulation	GMSK (BT = 0.3)	
Connection	8 ch/TDMA	
Voice digitizing	13 kbps RPE-LTP / 13 kps ACLEP / 5.6 kps CELP / VSLEP	
Transmission speed	270.3 kbps	
Diversity	Frequency hopping	
Signal Reception	Double superheterodyne	
Intermediate Frequencies	225 MHz and 45 MHz	
Antenna Terminal Impedance	50 Ω	
Antenna VSWR	<2.1 : 1	
Dimensions	Height: 120 mm Width: 45 mm Depth: 16.4 mm	
Volume	81 ml	
Weight	80 g	
Display	Graphical chip on glass liquid crystal, Alphanumeric, 16 x 4 characters + 2 lines of icons.	
Illumination	4 LEDs for the LCD (7-colour) 8 LEDs for the keypad (Green) 1 LED Incoming call (Green) 1 Charging LED (Red)	
Keys	18-key Keypad, Navigation key, Memo key.	
SIM	Plug-in type only	
External DC Supply Voltage	5.8 V	
Battery	3.7 V nominal, 650mAh, Li-Ion	
Standby Battery Life DRX 9	170 hrs maximum	
Conversation Battery Life PL 7, DTX 50%	210 minutes	

Battery life figures are dependent on network conditions.

WARNING

This service information is designed for experienced repair technicians only and is not designed for use by the general public. It does not contain warnings or cautions to advise non-technical individuals of potential dangers in attempting to service a product.
Products powered by electricity should be serviced or repaired only by experienced professional technicians. Any attempt to service or repair the product or products dealt with in this service manual by anyone else could result in serious injury or death.

Panasonic®

Issue 1
Revision 0

Company Liability

Comments or correspondence concerning this manual should be addressed to:

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Colthrop, Thatcham,

Berkshire, RG19 4ZD.
ENGLAND

CONTENTS

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1 INTRODUCTION

1.1. Purpose of this Guide

This Technical Guide contains technical information for the Panasonic GD93 personal cellular telephone operating on the GSM Digital Cellular Network.

1.2. Structure of the Guide

The manual is structured to provide service engineering personnel with the following technical information:

1. Interface details and relevant test points.
2. Functional description of each section of the mobile telephone.
3. Detailed description of each section of the mobile telephone.

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2 INTERFACES AND TEST POINTS

2.1. Interfaces

2.1.1 Main and Keypad PCBs

The interface between Main and Keypad PCBs is made via a 33-way connector.

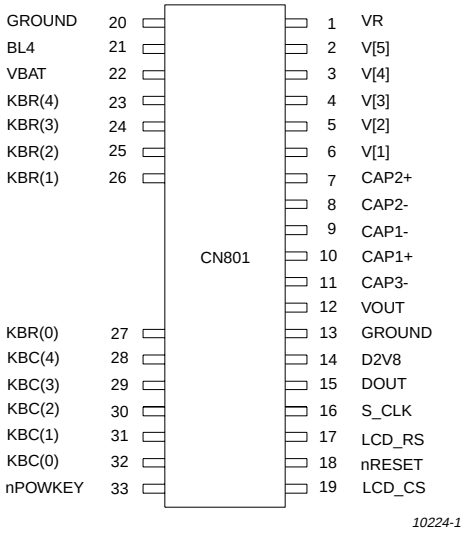


Figure 2.1: Interboard Connector

No.	Signal Name	MAIN <==> KEYPAD	Function	Connection
1	VR	==>	LCD Voltage Reference	
2	V[5]	==>	LCD Voltage Reference	
3	V[4]	==>	LCD Voltage Reference	
4	V[3]	==>	LCD Voltage Reference	
5	V[2]	==>	LCD Voltage Reference	
6	V[1]	==>	LCD Voltage Reference	
7	CAP2+		for LCD Stepup DC/DC	
8	CAP2-		for LCD Stepup DC/DC	
9	CAP1-		for LCD Stepup DC/DC	
10	CAP1+		for LCD Stepup DC/DC	
11	CAP3-		for LCD Stepup DC/DC	
12	VOUT			
13	GND		Ground	GND
14	D28VB		Power Source for LCD module	D28VB
15	DOUT		LCD control Serial data	HERCULES pin 5
16	S_CLK		LCD control Serial clock	HERCULES pin 12
17	LCD_RS	==>	LCD control Address data select	HERCULES pin 59
18	nRESET	==>	MPU nRESET signal	
19	CS.LCD	==>	LCD chip select signal	HERCULES pin 14
20	GND		Ground	GND
21	BL[4]		KEY Backlight	ACC IC #49
22	VBAT		Battery Voltage	
23	KBR(4)	<==	Key Row 4 signal for Key scan	HERCULES pin 179
24	KBR(3)	<==	Key Row 3 signal for Key scan	HERCULES pin 178
25	KBR(2)	<==	Key Row 2 signal for Key scan	HERCULES pin 176
26	KBR(1)	<==	Key Row 1 signal for Key scan	HERCULES pin 174
27	KBR(0)	<==	Key Row 0 signal for Key scan	HERCULES pin 173
28	KBC(4)	==>	Key Column 4 signal for Key scan	HERCULES pin 172
29	KBC(3)	==>	Key Column 3 signal for Key scan	HERCULES pin 171
30	KBC(2)	==>	Key Column 2 signal for Key scan	HERCULES pin 170
31	KBC(1)	==>	Key Column 1 signal for Key scan	HERCULES pin 169
32	KBC(0)	==>	Key Column 0 signal for Key scan	HERCULES pin 165
33	nPOWKEY	<==	Power Key sense signal	OMEGA pin 74

2.1.2 External I/O

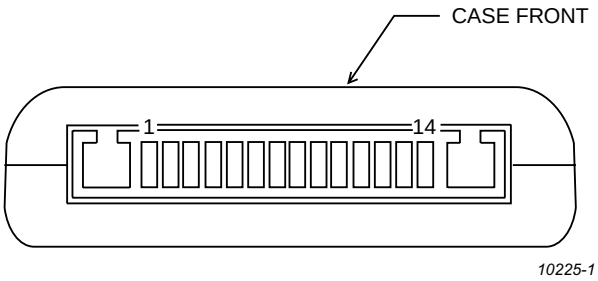
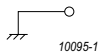
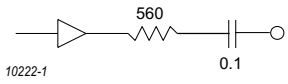
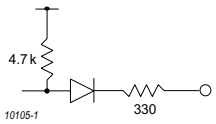
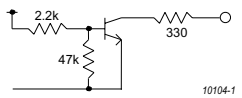
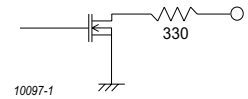
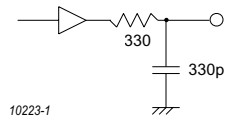
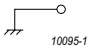


Figure 2.2: External I/O Connector

No.	Name	HH <==>EXT	Function	H/H Circuit
1	AGND	-	Audio Ground	
2	TX-AUDIO	<==	Sending Audio	
3	RX-AUDIO	==>	Received Audio	
4	VBAT IN / DATA_MODE0	<==	Battery Voltage Supply input / Data Accessory Recognition 0	
5	nACC_SENSE	<==	Handsfree / Data Accessory detection	
6	nAUDIO-ON	==>	Audio Path Control (L: On = un mute, Hi-Z: Off = mute)	
7	SERIAL UP	<==	Upward serial (9600 bps: SMS cable) (33.8 kbps: Data adaptor I/F Card) (up to 38.4 kbps: Soft Modem cable) (57.6 kbps: Test Command)	
8	SERIAL-DOWN	==>	Downward serial (Baud rate same as SERIAL-UP)	
9	ACC_PWR	==>	Peripheral power supply (on: less than 100 mA)	
10	DTR / DATA_MODE1	<==	RS232C: Data Terminal Ready / Data Accessory recognition 1	
11	RTS	<==	RS232C: Request to Send	
12	CTS / PA-ON	==>	PA control signal for test trigger (L: off, H 2.8V: on)	
13	EXT-PWR	<==	Power supply for Battery Charge	
14	GND	-	Power supply and digital signal ground	

2.1.3 SIM Interface

Pin	Signal
1	SIMPWR (3V / 5V)
2	SIM_RST
3	SIM_CLK
4	Not connected
5	Ground
6	Not connected
7	SIM-I/O
8	Not connected

2.2. Test Points

2.2.1 Main PCB

TP No.	Signal
TP601	nAUDIO_ON
TP602	DTR/DATA_MODE1
TP603	RTS
TP604	CTS/PA_ON
TP605	SERIAL_DOWN
TP606	SERIAL_UP
TP607	VBAT_IN/DATA_MODE0
TP608	KBR[4]
TP609	KBR[3]
TP610	KBR[2]
TP611	KBR[1]
TP612	KBR[0]
TP613	KBC[4]
TP614	KBC[3]
TP615	KBC[2]
TP616	KBC[1]
TP617	KBC[0]
TP618	nPOWKEY
TP619	SIM I/O
TP620	SIMCLK
TP621	SIM RST
TP622	SIMPWR
TP623	HERCULES TX_IRDA
TP624	HERCULES RX_IRDA
TP625	HERCULES CLK32_OUT
TP626	A28V
TP627	D28VB
TP628	D28V
TP629	D18V
TP630	D20V
TP631	EARP
TP632	EARN
TP633	BAT_TEMP
TP634	BAT_ID
TP635	HF_TXAUDIO
TP636	HF_RXAUDIO

TP No.	Signal
TP637	EXT_PWR
TP638	BL[1]
TP639	BL[2]
TP640	BL[3]
TP641	CHARGING_LED
TP642	PAGING_LED
TP643	VBAT
TP644	VBAT
TP645	U607 Pin 1 (32KOUT)
TP646	GROUND
TP647	GROUND
TP649	DTHFO_P
TP650	DTHFO_N
TP651	PHF_DET
TP652	HSRX_AUD
TP653	HSTX_AUD
TP654	E608 (MIC)
TP655	E607 (MIC)
TP656	n_ACC_SENSE
TP658	BL[4]
TP701	HERCULES TDI
TP702	HERCULES TDO
TP703	HERCULES TCK
TP704	HERCULES TMS
TP707	HERCULES nBSCAN
TP708	HERCULES SSDX
TP709	HERCULES SSDR
TP710	HERCULES SSCLK
TP711	HERCULES SSRST
TP712	OMEGA TESTRESET
TP713	OMEGA RESPWRONZ
TP715	OMEGA TDO
TP901	BACK_LED

2.2.2 Keypad PCB

TP No.	Signal
TP801	VBAT
TP802	DS801 / R801
TP803	DS802 / R801
TP804	DS803 / R802
TP805	DS804 / R802
TP806	DS805 / R803
TP807	DS806 / R803
TP808	DS807 / R804
TP809	DS808 / R804
TP810	nPOWKEY
TP811	KBR[0]
TP812	BL4
TP813	GROUND

3 RF OVERVIEW

3.1. Introduction

3.1.1 General Specifications

The telephone is a Dual Band product incorporating two switchable transceivers, one for the GSM 900 band and another for the GSM 1800 (DCS 1800) band. The transmit and receive bands for the mobile are given in the table below:

	Tx	Rx
GSM 900	890-915 MHz	935-960 MHz
GSM 1800	1710-1785 MHz	1805-1880 MHz

Other salient technical features are as follows:

	GSM 900	GSM 1800
Rx Bandwidth	25 MHz	75 MHz
Tx Bandwidth	25 MHz	75 MHz
Duplex Spacing	45 MHz	95 MHz
Number of Channels	124	374
AFRCN (Channel Numbers)	1-124	512-885
1st Tx Channel	890.2 MHz	1710.2 MHz
Last Tx Channel	914.8 MHz	1784.8 MHz
1st Rx Channel	935.2 MHz	1805.2 MHz
Last Rx Channel	959.8 MHz	1879.8 MHz
Maximum Tx Power	33.0 dBm (Class 4) (PL5)	30.0 dBm (Class 1) (PL0)
Minimum Tx Power	5.0 dBm (PL19)	0.0 (PL15)

3.1.2. Main PCB Description

All components required for the RF and Logic circuits, excluding the LCD module and backlight LEDs, are contained on the Main PCB. The Main PCB has six layers with an Any Layer Interstitial Via-Hole (ALIVH) structure which can connect from / to any layer. Surface and back layer tracks are gold-plated to prevent oxidisation and enable better soldering. The PCB thickness is 0.7 mm ±0.1 mm.

The majority of RF components are located on both sides of the top half area of the Main PCB. The Keypad PCB back layer consists mostly of groundplane which is used to provide RF shielding. A metallised plastic chassis has also been designed to provide smaller walled sections to isolate sensitive RF areas like the synthesiser block from high level interference such as the PA output and logic noise.

The back cover has a formed shielded enclosure to reduce further spurious emissions and logic noise.

3.2. Functional Description

3.2.1. Frequency Plan

The frequency plan is shown below:

	Tx	Tx IF	RFLO Tx	IFLO Tx
GSM 900	890 - 915 MHz	270 MHz	1160 - 1185 MHz	540 MHz
GSM 1800	1710 - 1785 MHz	135 MHz	1575 - 1650 MHz	540 MHz

	Rx	Rx 1st IF	Rx 2nd IF	RFLO Rx	IFLO Rx
GSM 900	935 - 960 MHz	225 MHz	45 MHz	1160 - 1185 MHz	540 MHz
GSM 1800	1805 - 1880 MHz	225 MHz	45 MHz	1580 - 1655 MHz	540 MHz

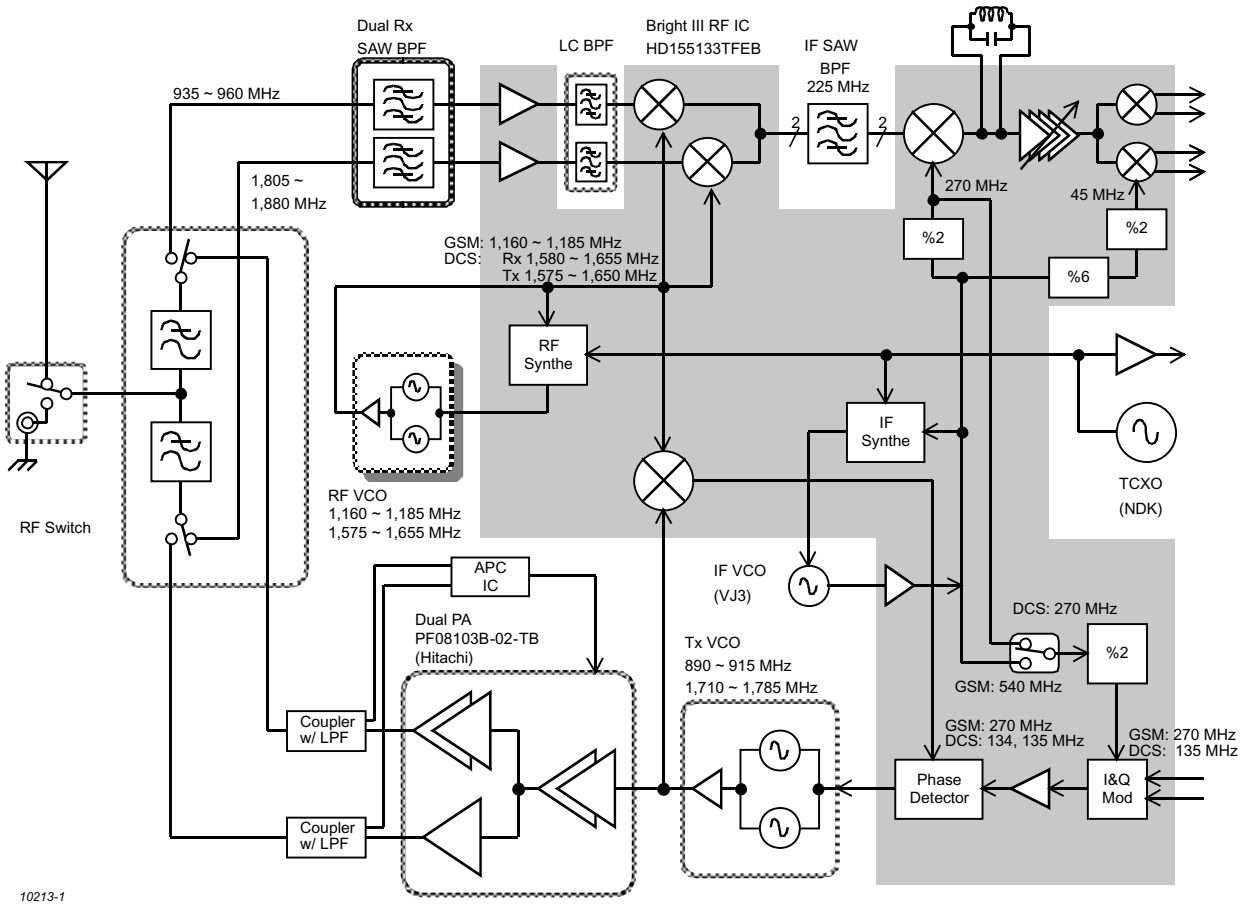


Figure 3.1: RF Block Diagram

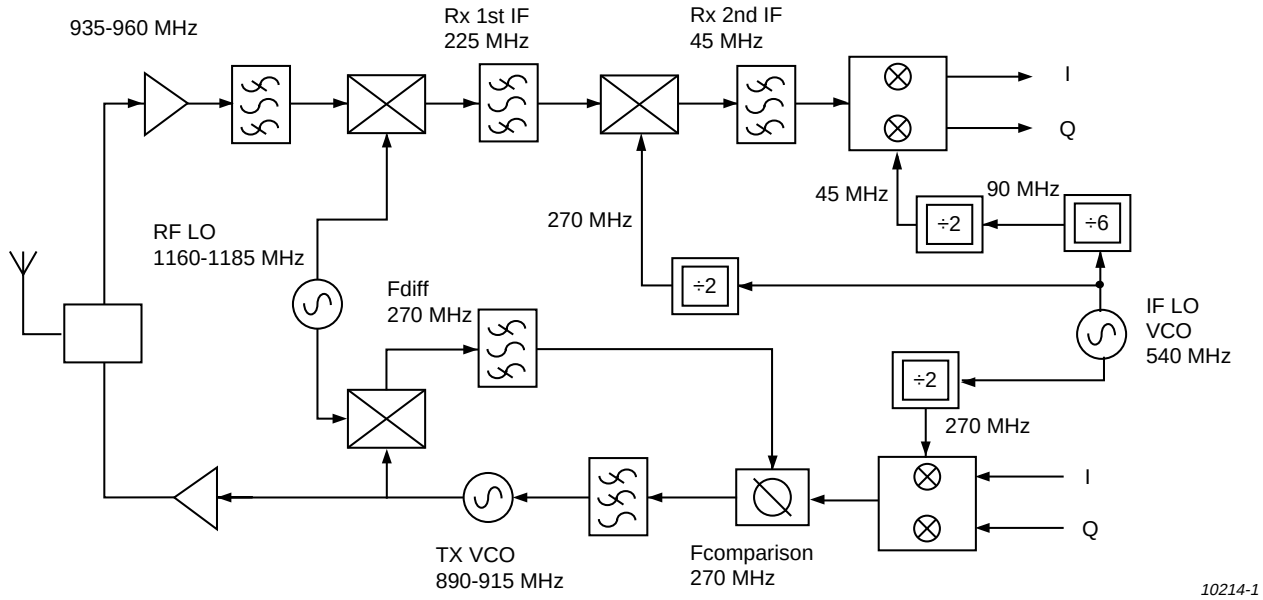


Figure 3.2: GSM 900 Frequency Plan

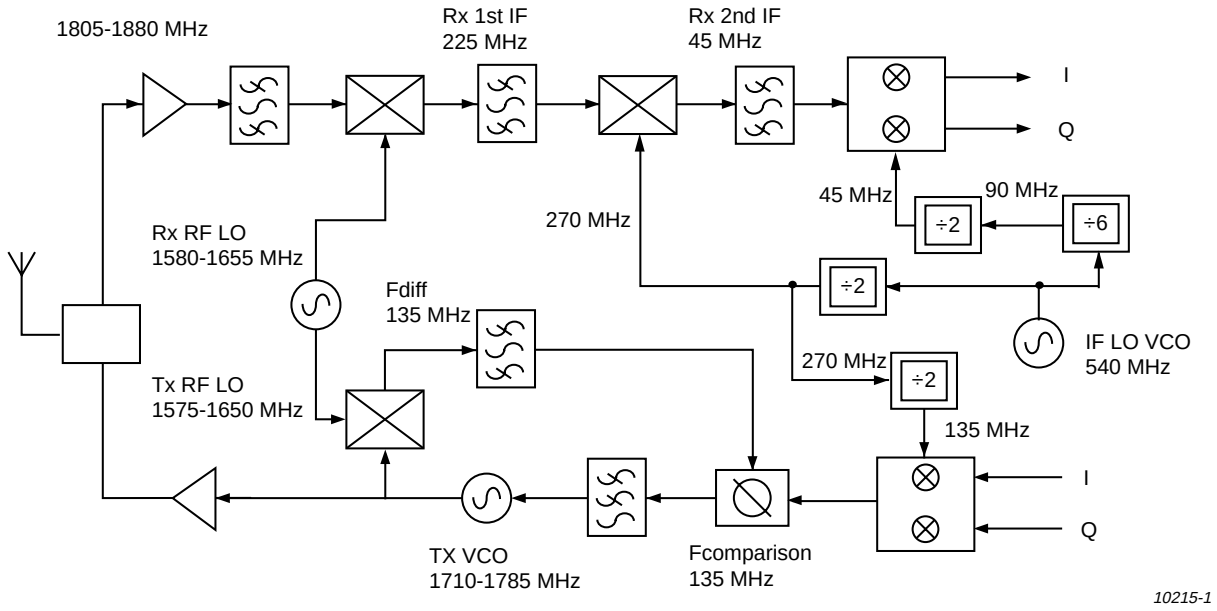


Figure 3.3: GSM 1800 Frequency Plan

3.2.2 General

The RF circuit design is built around an Hitachi Bright III GSM transceiver IC. Other major components include filters, power amplifiers, VCOs and the antenna subsystems.

In either band, GSM 900 or GSM 1800, the Rx IF is fixed at 225 MHz and the 2nd IF at 45 MHz. Therefore, the 2nd local oscillator is fixed at 540 MHz for receiver modes. This oscillator is also fixed at 540 MHz for transmit modes.

The Tx VCO is on-channel in both GSM 900 and GSM 1800 modes of operation.

3.2.3 Antenna

The antenna is a fixed helical type.

A mechanical switch is used to route the RF signal from the external antenna for handsfree operation and test purposes.

3.2.4 Transmit and Receive

The transmit and receive paths are covered in their own specific chapters later in this manual.

3.2.5 RF and Accessory Connector

An external antenna connector for use with handsfree accessories is located close to the PA module to minimise power loss. Therefore, the PAs do not have to be driven so hard, allowing the voltage supply to be lower, thus improving battery performance.

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4 TRANSMITTER

4.1. Introduction

This section provides a technical description of the transmitter circuits of the Main PCB. A circuit diagram of the whole system is provided in the Service Manual.

4.2. Uplink Frequencies

These assemblies MUST be performed by qualified service personnel at an authorised service centre.

The following Warnings and Cautions MUST be observed during all disassembly / reassembly operations:

4.2.1 GSM 900

The uplink frequencies for the GSM 900 band are as follows:

CHANNEL NUMBERS	UPLINK FREQUENCIES				
1-5	890.200	890.400	890.600	890.800	891.000
6-10	891.200	891.400	891.600	891.800	892.000
11-15	892.200	892.400	892.600	892.800	893.000
16-20	893.200	893.400	893.600	893.800	894.000
21-25	894.200	894.400	894.600	894.800	895.000
26-30	895.200	895.400	895.600	895.800	896.000
31-35	896.200	896.400	896.600	896.800	897.000
36-40	897.200	897.400	897.600	897.800	898.000
41-45	898.200	898.400	898.600	898.800	899.000
46-50	899.200	899.400	899.600	899.800	900.000
51-55	900.200	900.400	900.600	900.800	901.000
56-60	901.200	901.400	901.600	901.800	902.000
61-65	902.200	902.400	902.600	902.800	903.000
66-70	903.200	903.400	903.600	903.800	904.000
71-75	904.200	904.400	904.600	904.800	905.000
76-80	905.200	905.400	905.600	905.800	906.000
81-85	906.200	906.400	906.600	906.800	907.000
86-90	907.200	907.400	907.600	907.800	908.000
91-95	908.200	908.400	908.600	908.800	909.000
96-100	909.200	909.400	909.600	909.800	910.000
101-105	910.200	910.400	910.600	910.800	911.000
106-110	911.200	911.400	911.600	911.800	912.000
111-115	912.200	912.400	912.600	912.800	913.000
116-120	913.200	913.400	913.600	913.800	914.000
121-124	914.200	914.400	914.600	914.800	

Uplink frequencies for the GSM 900 band can be calculated as follows:

Uplink frequency = 890 MHz + (ARFCN x 0.2 MHz)
e.g. for CH55
890 MHz + (55 x 0.2 MHz)
= 890 MHz + (11 MHz)
= 901 MHz

4.2.2. GSM 1800

The uplink frequencies for the GSM 1800 band can be calculated as follows:

Uplink frequency = 1710 MHz + ((AFRCN - 511) x).2MHz)
e.g. for CH512
1710 MHz + ((512 - 511) x 0. 2MHz)
= 1710 MHz + (0.2 MHz)
= 1710.2 MHz

4.3. Functional Description

4.3.1 Circuit Description

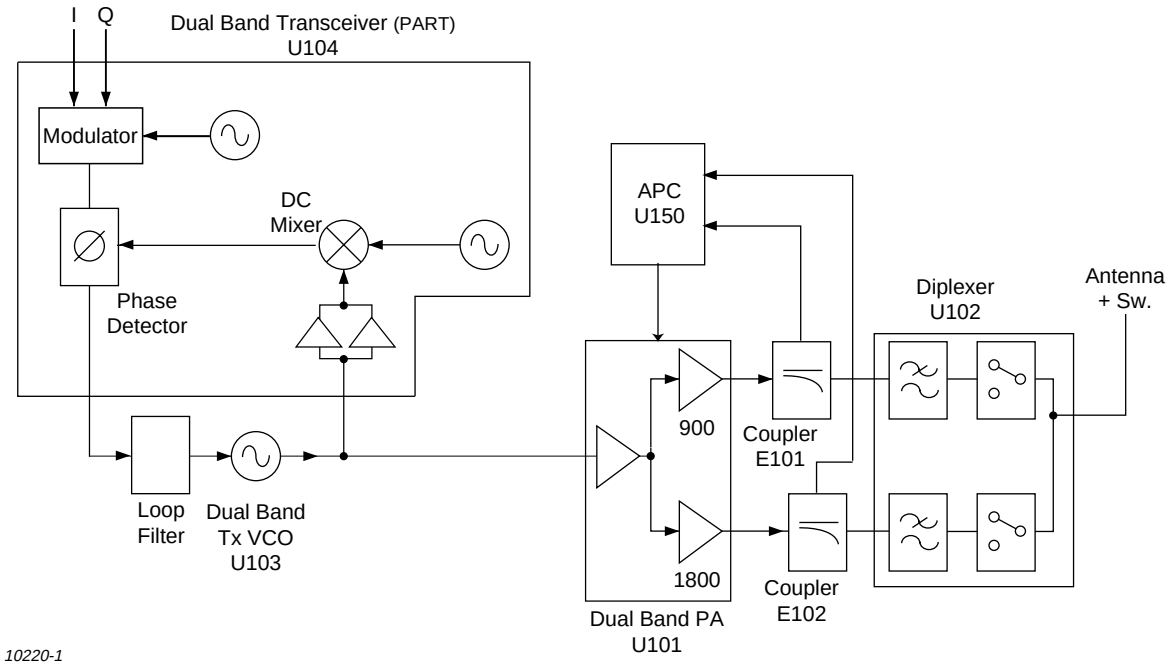

Figure 4.1: Transmitter Block Diagram

The transmitter design is based on an IQ Modulator and operates at Class 4 (2W) in the GSM 900 band and at Class 1 (1W) in the GSM 1800 band. The architecture has been carefully chosen to limit GSM transmitter noise in the receiver band without the requirement for a duplexer.

The RF IC Bright III (U104) provides the following transmitter functions:

- I, Q Quadrature modulator
- Down conversion mixer for modulated signal to intermediate frequency.
- Phase detector for PLL modulation loop.

The IF LO signal generated by the IF VCO is modulated by the baseband I, Q signals in the quadrature modulator. Output from the quadrature modulator is fed into the phase detector for the PLL modulation loop.

The output from the Tx VCO is fed in to the down conversion mixer. It is mixed with the 1st LO output (from the RF VCO) and converted to the IF frequency.

The charge pump output signal produced by the phase detector is fed back to the Tx VCO to generate modulated RF output.

The Tx VCO has been designed to provide a high level output thus obviating the need for a driver amplifier. Therefore, the Tx VCO output is applied directly to the PA which amplifies the signal to any required level up to PL5 (33 dBm at the antenna) for GSM 900 and PL0 (30 dBm) for GSM 1800. The output from the PA is fed to a low-pass filter within the directional coupler to ensure that there is sufficient margin in the rejection of second and third harmonics.

4.3.2. GSM 900 Signal Levels

The transmitter signal levels for the GSM 900 band are as follows:

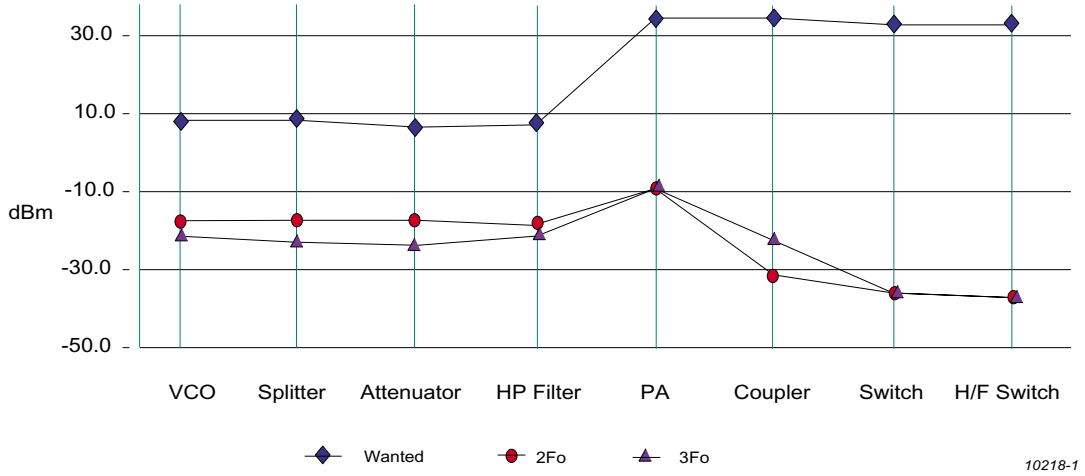

Figure 4.2: GSM 900 Transmitter Signal Levels

4.3.3. GSM 1800 Signal Levels

The transmitter signal levels for the GSM 1800 band are as follows:

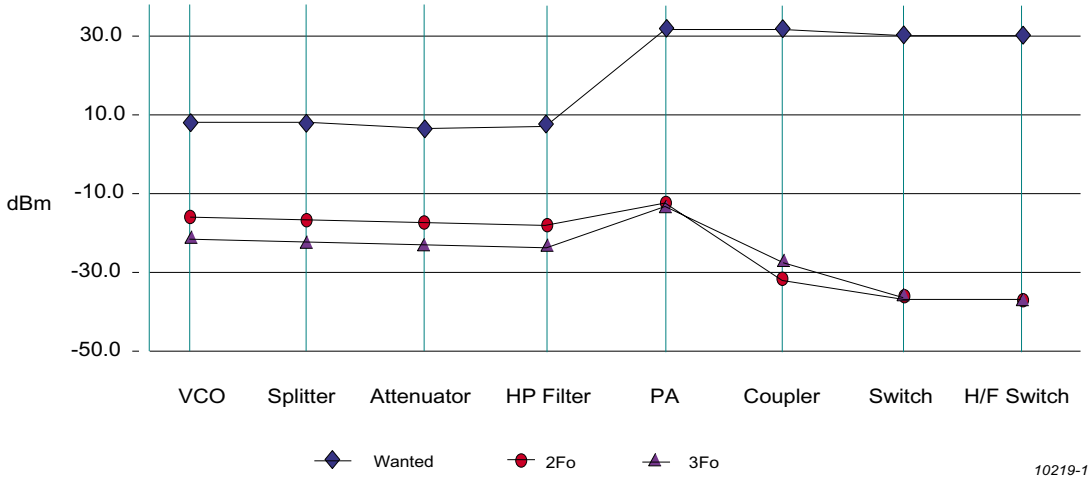

Figure 4.3: GSM 1800 Transmitter Signal Levels

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5 RECEIVER

5.1. Introduction

This Section provides a technical description of the receiver section of the Main PCB. A complete circuit diagram is provided in the Service Manual.

5.2. Downlink Frequencies

5.2.1. GSM 900

The downlink frequencies for the GSM 900 band are as follows:

CHANNEL NUMBERS	DOWNLINK FREQUENCIES (MHz)				
1-5	935.200	935.400	935.600	935.800	936.000
6-10	936.200	936.400	936.600	936.800	937.000
11-15	937.200	937.400	937.600	937.800	938.000
16-20	938.200	938.400	938.600	938.800	939.000
21-25	939.200	939.400	939.600	939.800	940.000
26-30	940.200	940.400	940.600	940.800	941.000
31-35	941.200	941.400	941.600	941.800	942.000
36-40	942.200	942.400	942.600	942.800	943.000
41-45	943.200	943.400	943.600	943.800	944.000
46-50	944.200	944.400	944.600	944.800	945.000
51-55	945.200	945.400	945.600	945.800	946.000
56-60	946.200	946.400	946.600	946.800	947.000
61-65	947.200	947.400	947.600	947.800	948.000
66-70	948.200	948.400	948.600	948.800	949.000
71-75	949.200	949.400	949.600	949.800	950.000
76-80	950.200	950.400	950.600	950.800	951.000
81-85	951.200	951.400	951.600	951.800	952.000
86-90	952.200	952.400	952.600	952.800	953.000
91-95	953.200	953.400	953.600	953.800	954.000
96-100	954.200	954.400	954.600	954.800	955.000
101-105	955.200	955.400	955.600	955.800	956.000
106-110	956.200	956.400	956.600	956.800	957.000
111-115	957.200	957.400	957.600	957.800	958.000
116-120	958.200	958.400	958.600	958.800	959.000
121-124	959.200	959.400	959.600	959.800	

Downlink frequencies for the GSM 900 band can be calculated as follows:

Downlink frequency = 935 MHz + (ARFCN x 0.2 MHz)
e.g. for CH55
935 MHz + (55 x 0.2 MHz)
= 935 MHz + (11 MHz)
= 946 MHz

5.2.2. GSM 1800

The downlink frequencies for the GSM 1800 band can be calculated as follows:

Downlink frequency = 1805 MHz + ((ARFCN - 511) x 0.2 MHz)
e.g. for CH512
1805 MHz + ((512 - 511) x 0.2 MHz)
= 1805 MHz + (0.2 MHz)
= 1805.2 MHz

5.3. Functional Description

5.3.1. Dual Band Receiver IC

The main building block for the Dual Band receiver is the Hatchi Bright III GSM transceiver IC (U104). The receiver is a superheterodyne type with the 1st IF at 225 MHz and 2nd IF at 45 MHz. The intermediate frequencies are common to both frequency bands.

The receiver section of U104 contains the following stages:

- Dual band LNA stage.
- Gain controlled 1st mixer for GSM 900 band.
- Gain controlled 1st mixer for GSM 1800 band.
- Gain controlled 2nd mixer.
- Gain controlled IF amplifier.
- I, Q quadrature down converter.
- Baseband operational amplifiers for further amplification and some filtering of the baseband I, Q signals.

5.3.2. Circuit Description

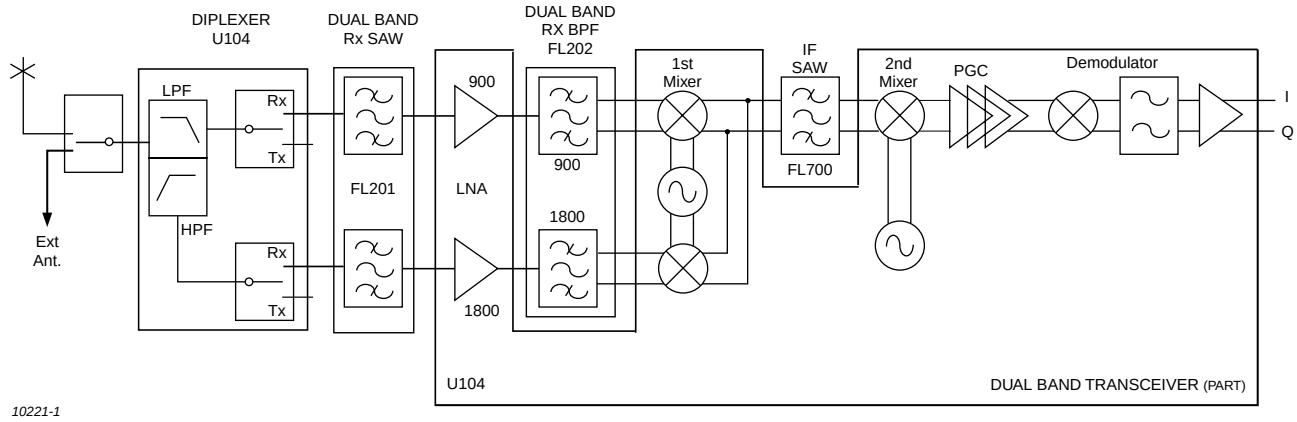

Figure 5.1: Dual Band Receiver

RF input to the receiver is either via the antenna or via the external antenna connector. The input signal from the antenna is fed into the GSM 900 / GSM 1800 dual band Antenna switch module which comprises a diplexer and diode switches. The diplexer splits the two GSM frequency bands whilst the pin switches route the signal flow from the receiver and the transmitter as required.

The output is applied to the 1st dual band receiver SAW filter which provides the roofing filter for the Rx front end for both 900 MHz and 1800 MHz bands. Note that the apprpriate signal path will be set by the Antenna switching module. The output is applied to the internal dual LNA of the Bright III IC.

The Bright III LNA gain is constant, typical gain is +17 dB for GSM 900 and +16 dB for GSM 1800, with a typical noise factor of 1.5 dB and 1.7 dB respectively.

The output from the dual LNA passes through a dual LC filter which is designed to reduce interference at image spurious frequency, and is fed into the 1st mixer of each band. Both 1st mixers are gain controlled by 3-wire bus to (typically) between +9.5 dB and -1.0 dB for GSM 900 and between +8.5 dB and -4.0 dB for GSM 1800.

The 1st IF output at 225 MHz is filtered by the differential IF SAW filter to reduce adjacent channel interference before application to the 2nd mixer. The use of differential filters eliminates the need for a balun transformer, providing some cost and space advantage.

The 2nd mixer is also gain controlled by 3-wire bus between, typically, +13.0 dB and -3.0 dB. Gain switching is synchronised with the 1st mixer. The 2nd mixer output at 45 MHz is filtered by an L-C network before it is applied to the IF amplifier.

The IF amplifier is gain controlled by 3-wire bus for AGC purposes. The gain can be adjusted between -29 dB and +69 dB in 2 dB steps.

IF amplifier output is fed into two quadrature mixers where it is converted down to baseband. The IF LO is generated at 540 MHz using an external VCO module. An on-chip divider on the Bright III IC divides this signal by six and then by two. It also produces two outputs in quadrature to generate the baseband I and Q signals. The outputs from the mixers are connected to external pins through a pair of buffers. Two on-chip operational amplifiers are used to amplify the AC signal from the mixers.

The DC level at the output of the operational amplifiers is 1.35 V with a 200 mV p-p single-ended AC swing controlled by the AGC loop to maintain optimum receiver signal levels.

5.3.3. GSM 900 Signal Levels

The receiver signal levels for GSM 900 band are given below:

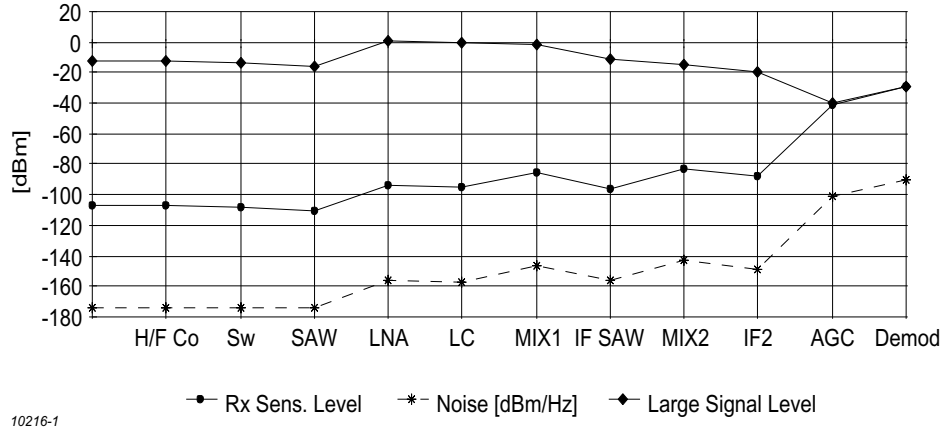

Figure 5.2: GSM 900 Receiver Signal Levels

5.3.4. GSM 1800 Signal Levels

The receiver signal levels for GSM 1800 band are given below:

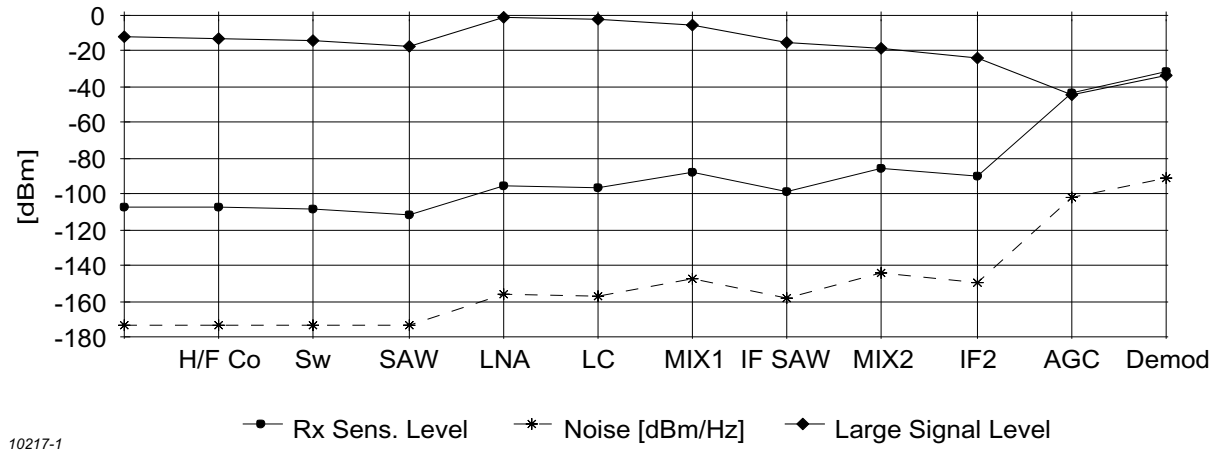

Figure 5.3: GSM 1800 Receiver Signal Levels

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6 BASEBAND OVERVIEW

6.1. Introduction

The main Baseband circuitry is located within the RF circuits on the Main PCB, while the keypad, LCD and backlights are located on the Keypad PCB.

A metallised plastic chassis is used to separate the Main and Keypad PCBs. The continuous chassis design is important for EMC purposes. When the chassis is sandwiched between the two PCB assemblies, the groundplane of the Keypad PCB together with the chassis forms an effective shielded enclosure, preventing spurious emissions.

The baseband circuit utilises a two-chip GSM chipset developed by Texas Instruments. One chip (HERCULES) carries out signal processing with DSP and CPU, and the second chip (OMEGA) contains the analogue interface and power control.

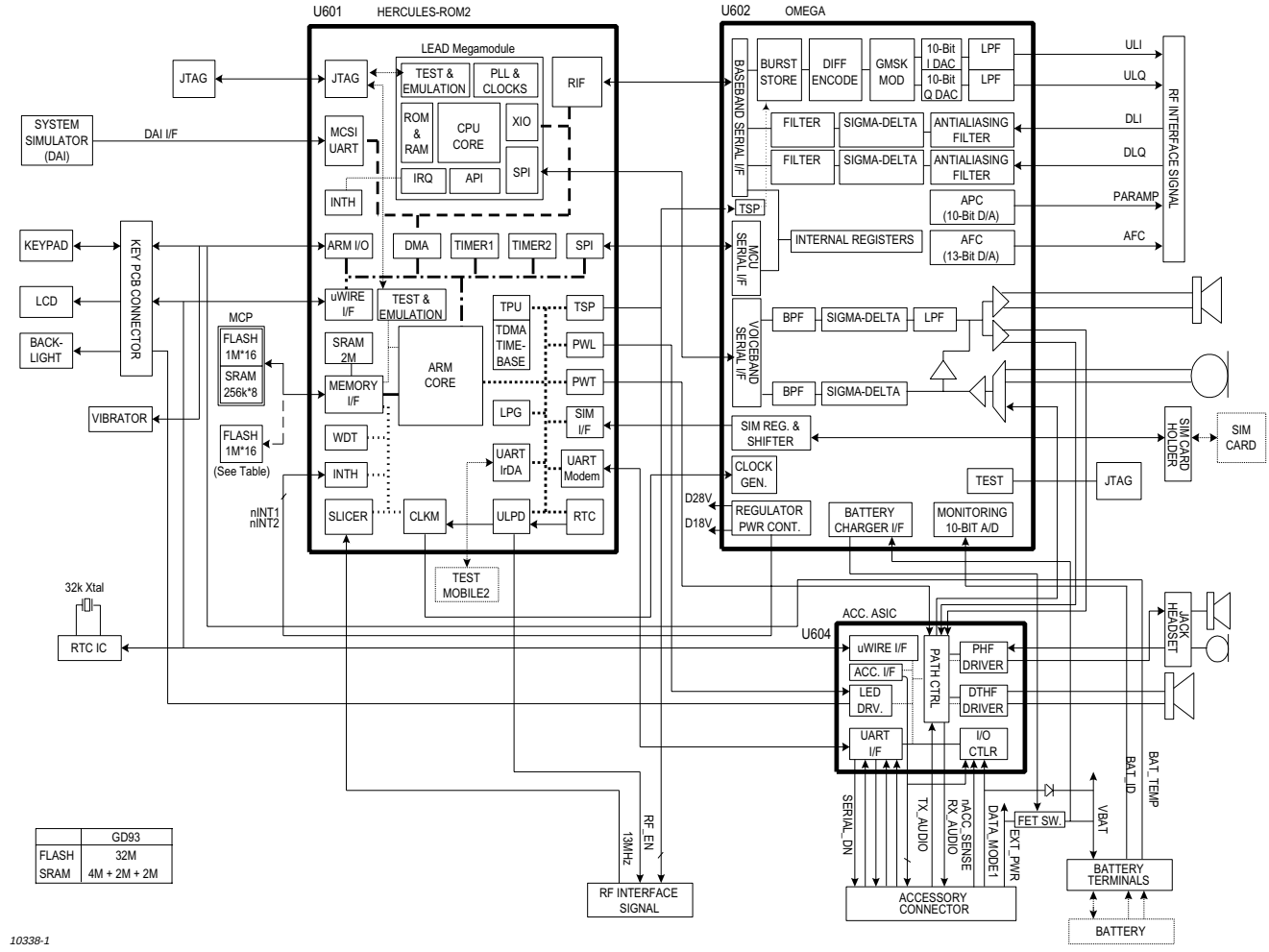

Figure 6.1: Baseband Block Diagram

6.2. Keypad

The Keypad has a 5 x 5 matrix, allowing 25 keys to be scanned. When a key being pressed, a keypad interrupt is generated. To find which key has been pressed, the software asserts each column in turn and reads which row is active. Because of key-bounce, the key press is confirmed by reading the row again approximately 20ms later.

As the End Key doubles for the ON/OFF key, it is allocated an entire row of the keyboard scan.

The Keyboard scanning is software controlled, Key pressed is indicated by an interrupt, but key release is controlled by software.

6.3. Subscriber Identity Module (SIM)

The SIM interface is designed to support 3 V and 5 V SIMs.

HERCULES operates from a 2.85 V supply. OMEGA has level translators for 3 V and 5 V SIMs.

$FFFE:0000	REG_SIM_CMD	SIM control register	Write only
$FFFE:0002	REG_SIM_STAT	SIM status register	Read only
$FFFE:0004	REG_SIM_CONF1	SIM configuration register 1	Read/Write
$FFFE:0006	REG_SIM_CONF2	SIM time delay parameters	Read/Write
$FFFE:0008	REG_SIM_IT	SIM Interrupt status	Read only
$FFFE:000A	REG_SIM_DRX	SIM receive byte register	Read only
$FFFE:000C	REG_SIM_DTX	SIM transmit byte register	Read/Write
$FFFE:000E	REG_SIM_MASKIT	SIM interrupt mask register	Read/Write

6.4. Time Processing Unit (TPU)

The TPU provides the GSM TDMA timing requirements for the system, external timing signals are provided by an area of Microcode within OMEGA.

TPU Timing output signal assignments of HERCULES

Name	PIN No.	Function	Connection	Configuration
TSPACT 0	133	TXON1	RF	
TSPACT 1	135	NC	N/A	
TSPACT 2	137	NC	N/A	
TSPACT 3	139	VCO_EN	RF	
TSPACT 4	145	PA_ON	Acc IC	
TSPACT 5	148	PCNnGSM	RF	
TSPACT 6	153	DCS_PAON	RF	
TSPACT 7:CLKX_SPI	162	GSM_PAON	RF	Asic_conf_reg[9] = 0
TSPACT 8:nMREQ	166	NC	N/A	
TSPACT 9:MAS1	167	NC	N/A	
TSPACT 10:nWAIT	108	NC	N/A	
TSPACT 11:MCLK	101	NC	N/A	

$FFFE:1000	REG_TPU_CTRL	Control/Status register	Read/Write
$FFFE:1002	REG_INT_CTRL	Interrupt control register	Write only
$FFFE:1004	REG_INT_STAT	Interrupt status register	Read only
$FFFE:100C	REG_TPU_OFFSET	Offset register	Read only
$FFFE;100E	REG_TPU_SYNCHRO	Synchronous register	Read only
$FFFE:1020	RE_IT_DSPPG	DSP Programmable IT	Write only

6.5. CPU Memory

To accommodate the memory requirements of the WAP browser, the telephone uses large memory Flash and SRAM with the following configuration:

- 32 Mbits Flash memory organised as 2 M * 16
  4 Mbits RAM organised as 256k * 16 plus 128k * 16 plus 128k * 16
- The 8 Mbits RAM consists of 2 Mbits HERCULES internal RAM, 2 Mbits external RAM only, and 2 Mbits external RAM on MCP.

6.6. LCD

The LCD modules consists of a LCD glass and driver chip on a flexible PCB with connection to the Main PCB.

The LCD has a format of 96 x 65 pixels to provide maximum information. It can display up to three lines of 16 characters plus two lines of icons.

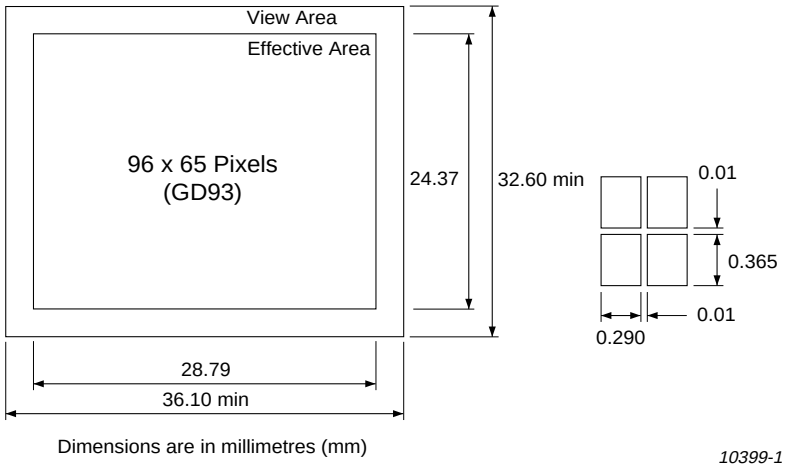

Figure 6.2: LCD Dimensions

The LCD is driven by an EPSON SED1565 display driver which has internal RAM for the display. The driver is controlled by setting the command register through the Hercules uwire I/F and one I/O line assigned to distinguish command or data. When sending data or commands, the nSCS0 line is used for chip select. To send data, LCD_RS(I/O 3) is set high, and to send commands, the line is set low.

6.7. Real Time Clock (RTC)

Clock functions are provided by an external Real Time Clock module (U607). The module is synchronised by a 32.768kHz crystal and has a back-up power source provided by a button battery.

A clock auto compensation function calibrates crystal frequency tolerance by writing compensation registers. Calibration range is ± 555.6 ppm in 0.0085 ppm steps.

6.8. Microphone

To provide improved speech pick-up, noise immunity and reduced echo, the microphone is a noise cancelling type which requires a FLIP for acceptable frequency response. The GSM Standard requires that when in handheld mode, the transmitter audio frequency response must fit within the mask shown below:

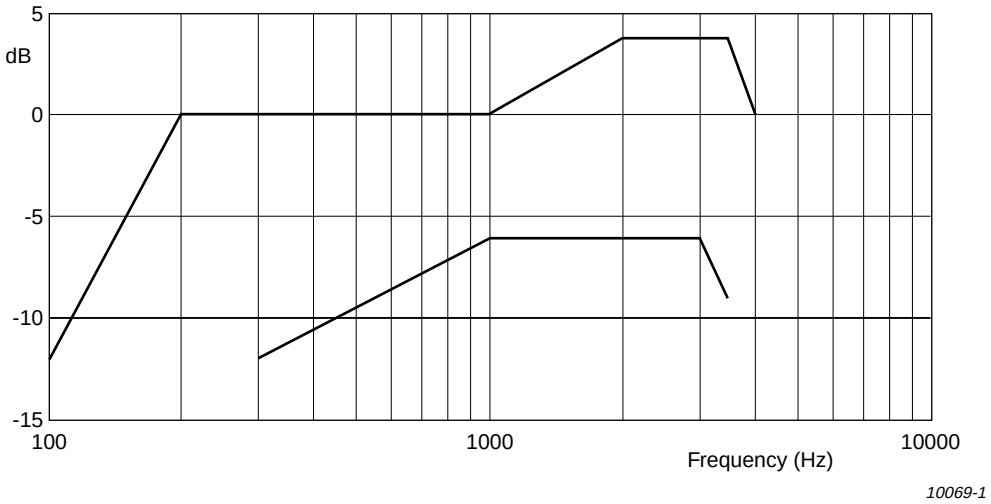

Figure 6.3: Handheld GSM Transmit Audio Frequency Response Mask

When using a Handsfree accessory, the GSM Standard requires that the transmitter audio frequency response must fit within the mask shown below:

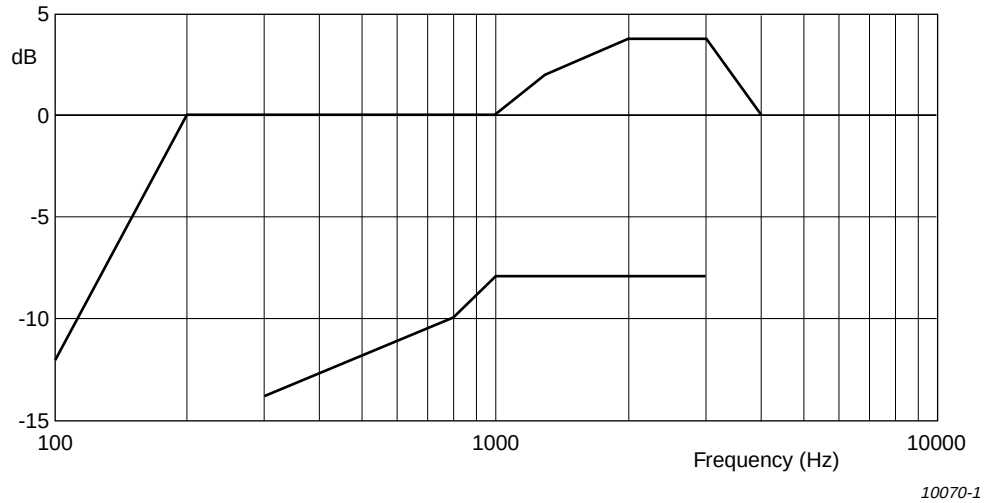

Figure 6.4: Handsfree GSM Transmit Audio Frequency Response Mask

6.9. Speaker

6.9.1. Handheld Mode

Because OMEGA is powered from a 2.7 V supply, a low impedance (dynamic) speaker must be used. The GSM Standard requires that the receiver audio frequency response must fit within the mask shown below.

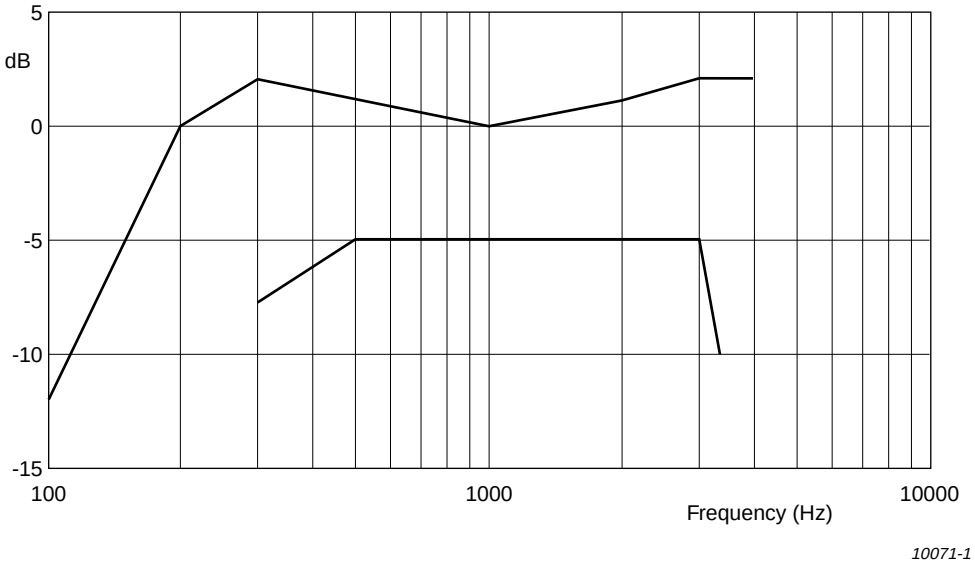

Figure 6.5: Handheld GSM Receive Audio Frequency Response

The telephonehas been designed to meet requirements with a Type 1 artificial ear.

Volume Levels			
Volume Level	**PGA**	**Volume**	**Total Gain**
1	+1 dB	0 dB	+1 dB
2	-2 dB	0 db	-2 dB
3	-5 dB	0 dB	-5 dB
4	-5 dB	-6 dB	-11 dB

6.9.2. Desktop Handsfree (DTHF)

A second speaker is mounted in the rear case for DTHF operation. The GSM Standard requires that the receiver audio frequency response must fit within the mask shown below.

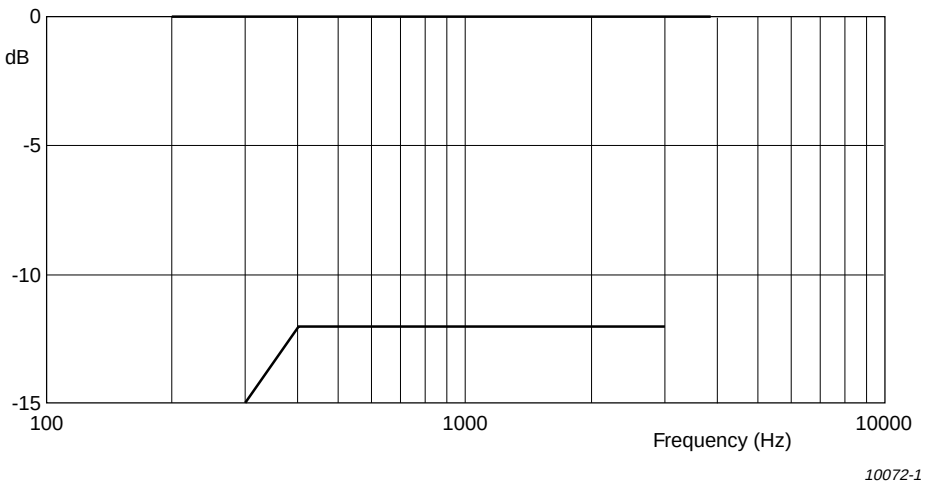

Figure 6.6: Handsfree GSM Receive Frequency Response Mask

Ringing Tones are played through the DTHF speaker. The volume level of ringing tones is defined by the 6-bit PWM register setting in HERCULES I/O and by the ASIC IC.

Timer 1 in HERCULES is used to time the period between switching the ringing on, and off to make the tone. For more complex buzzer ringing tones, the buzzer volume level can also be altered after each time-out of Timer 1.

6.10. Timers

A watchdog timer and two 16-bit general purpose timers can be used either as auto-reload or one-shot timers to provide interrupts to the ARM CPU. A prescaler and 16-bit register define the timer clock duration. The watchdog timer receives 928 kHz clock signal from the HERCULES clock module. A combination of prescaler and timer register gives a time range of 1.078 μs and 9.039 s.

The general purpose timers unit receive a 812.5 kHz clock signal. Timer range is between 2.4615 μs and 20.649 s.

Timer 1	Function	=	Buzzer Timer *
	Setting	=	Tone frequency *
Timer 2	Function	=	N/A
	Setting	=	N/A

The timer unit registers are.

$FFFF:F800	Watchdog_CNTL_TIM	Watchdog control	6 bit	Read/Write
$FFFF:F802	Watchdog_LOAD_TIM	Load Watchdog	16 bit	Write only
$FFFF:F802	Wartchdog_READ_TIM	Read Watchdog	16 bit	Read only
$FFFF:F804	Watchdog_TIM_MODE	Watchdog Mode	9 bit	Read/Write
$FFFE:3800	CNTL_TIMER1	Control timer1	8 bit	Read/Write
$FFFF:3802	LOAD_TIM1	Load Timer 1	16 bit	Read/Write
$FFFF:3804	READ_TIM1	Read Timer 1	16 bit	Read only
$FFFE:6800	CNTL_TIMER2	Control timer2	8 bit	Read/Write
$FFFF:6802	LOAD_TIM2	Load Timer 2	16 bit	Read/Write
$FFFF:6804	READ_TIM2	Read Timer 2	16 bit	Read only

6.11. UART

Hercules has two UART ports, UART/modem and UART/IrDA. Only the UART/modem port is used. UART/IrDA port can be used for software debug purposes.

USART Pin Assignments			
Signal Name	**Pin No.**	**Function**	**I/O**
TXD	7	UART Serial Tx Data	O
RXD	6	UART Serial Rx Data	I
DSR	9	UART Data Terminal Ready	I
RTS	10	UART Ready to Send	O)
CTS	11	UART Clear To Send	I

Registers for UART are located as follows:

$FFFF:5000 to $FFFF:5011	UART/IrDA
$FFFF:5800 to $FFFF:5811	UART/modem

6.12. Accessory ASIC

6.12.1. General Information

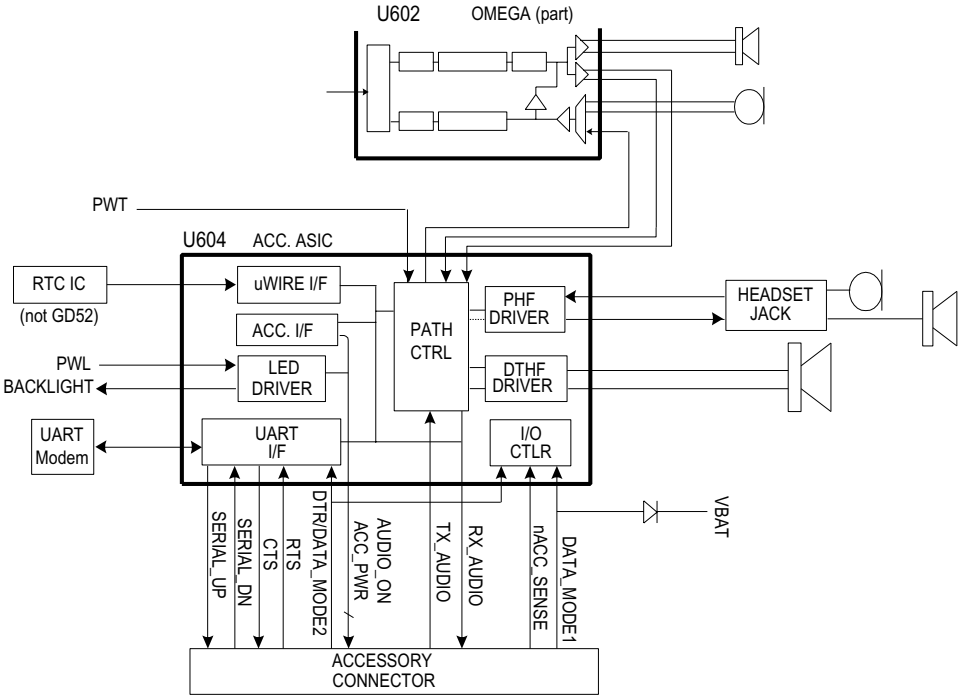

Figure 6.7: Accessory ASIC (U604)

The Accessory ASIC (U604) consists of the following:

- LED drivers
- BUZZER driver
- Level shifter for UART interface
- Accessory control I/O lines
- Audio drives

6.12.2. Registers

The Accessory ASIC is controlled by setting registers through the Hercules UART interface.

The Control block contains four registers accessed via the serial interface.

R0, R1 and R2 are 8-bit write only registers
R3 is an 8-bit read-only register

Serial Interface bit	Bit function R0	Bit function R1	Bit function R2	Bit function R3
R/W	0	0	0	1
A1	0	0	1	1
A0	0	1	0	1
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
D7	PAGING_LED	Not used	AUDIO_ON	SENSE0

Serial Interface bit	Bit function R0	Bit function R1	Bit function R2	Bit function R3
D6	CHARGING_LED	Not used	PWM_ON	nPHF_DETECT
D5	BLCONT4	DTHF ON	EN_UART	SENSE1
D4	BLCONT3	HF_SELECT	BUCONT4	SENSE1
D3	BLCONT2	HF_RX_ON	BUCONT3	AUDIO_CONT1
D2	BLCONT1	HF_TX_ON	BUCONT2	AUDIO_CONT0 (nACC_SENSE)
D1	PA_ON_SEL	MIC_BIAS	BUCONT1	DATA_MODE1
D0	LOGIC_POWER	HF_MUTE	BUCONT0	DATA_MODE0
RESET VALUE	00 hex	00 hex	00 hex	-

6.12.3. Path Control

To avoid switching noise, switching of HF_RX_ON bit is performed while HF_MUTE is enabled. HF_MUTE is released 80ms - 120ms after HF_RX_ON goes high and muted 80ms - 120ms before HF_RX_ON goes low.

The HF_MUTE signal is controlled when H/H operates DTHF and PHF.

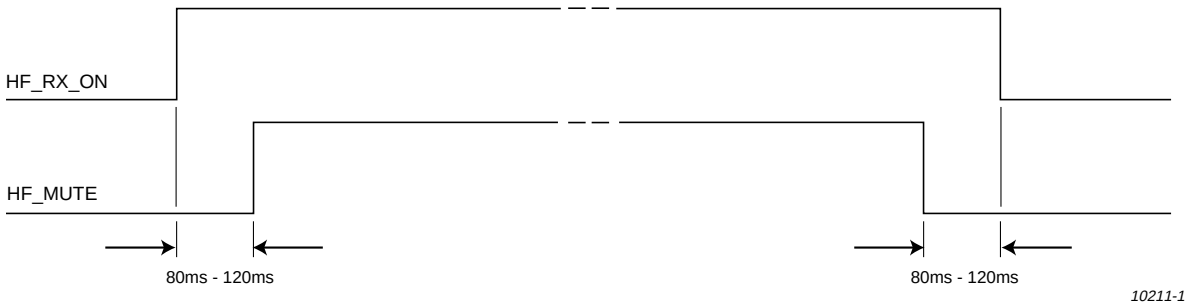

Figure 6.8: Path Control

6.12.4. LED Control

The LCD backlight is illuminated by controlling BLCONT1 to BLCONT4 as follows:

	Red Type 1	Green Type 2	Magenta Type 3	Light Blue Type 4	Type 5	Type 6	Type 7
BLCONT1	0	1	1	1	0	0	1
BLCONT2	1	0	1	0	1	0	1
BLCONT3	1	0	0	1	0	1	1
BLCONT4	0	1	0	0	0	1	0

6.12.5. Accessory Control

The DATA_MODE1, DATA_MODE2 and AUDIO_CONT1 bits are able to read 1 ms after LOGIC_PWR bit is set to ‘1’. This delay time is dependant on the ACC_PWR capacitance of the connected accessory.

7 HERCULES

7.1. Introduction

Hercules contains the DSP, CPU and GSM timing functions, and many peripheral functions. The software for the DSP is contained in masked ROM.

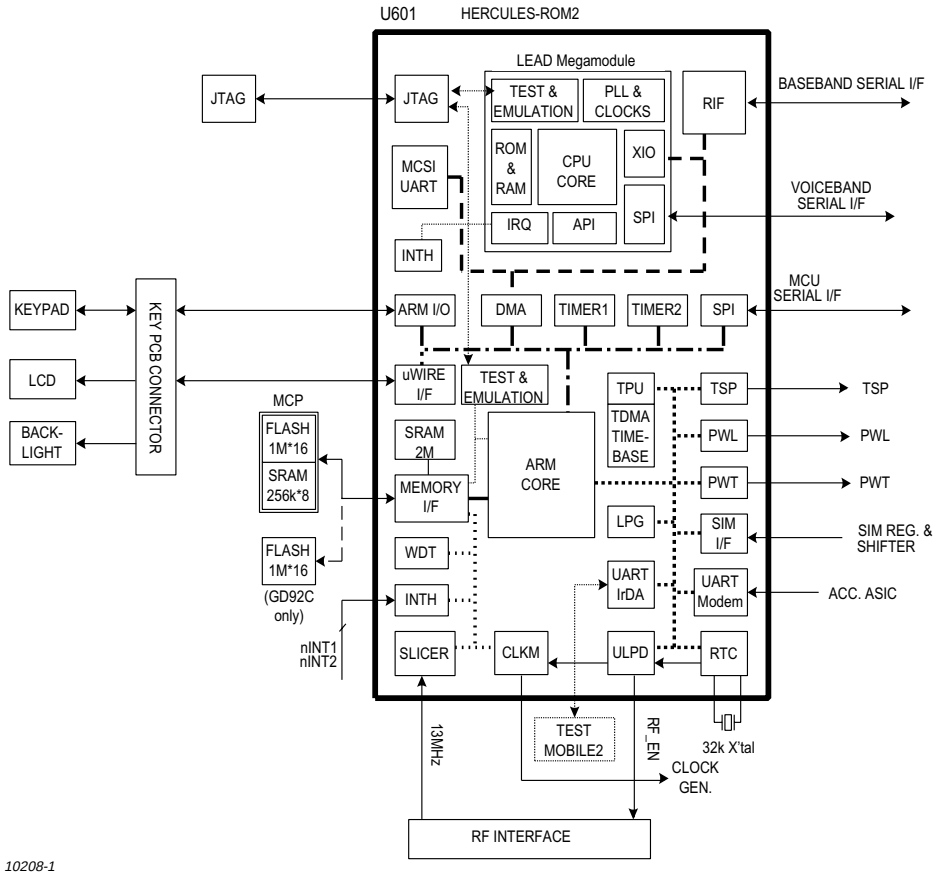

Figure 7.1: HERCULES Block Diagram

7.2. Digital Signal Processor

The Digital Signal Processor (DSP) core is compatible with a GSM chipset designed by Texas Instruments. Included in the DSP core is an interface to the CPU by a shared memory interface.

The DSP memory is also located within HERCULES. The ROM code size is determined by the size of the software.

7.3. CPU

The CPU is an ARM7 32-bit RISC CPU with 16-bit instruction set. The CPU is designed to access 32-bit memory and peripherals, a further module within the HERCULES chip allows access to 8 or 16-bit memory. CPU clock speed is selectable and is set to achieve optimum speed for memory access.

Memory Access Times		
Clock Speed	**Memory Access Time**	**Additional Access time per wait state**
13 MHz	67 ns	77 ns
8.67 MHz	105 ns	115 ns
6.5 MHz	144 ns	154 ns‘3
3.25 MHz	298 ns	308 ns

For 90 ns access FLASH and RAM, a 8.67 MHz clock gives no wait state access to both devices. Debugging access for the CPU is provided via the JTAG interface.

7.4. Memory Interface

The memory interface allows the 32-bit CPU access to 16 and 8-bit devices, and allows the addition of wait states to memory access. The memory interface allows between 0 and 31 wait states to be added. The ROM area is hardware write-protected, a FLASH write enable bit in the ROM wait state configuration register can be used to enable write access to the ROM area.

CPU Memory Map					
Device Name	**Start Address**	**Size**	**Function**	**Bus width**	**Wait States**
ROM	0000:0000	8M	FLASH 2M bytes	16 bits	0
nCS1	0080:0000	8M	Static RAM 256k bytes *	16 bits	0
nCS2	0100:0000	8M	not used	16 bits	0
nCS3	0180:0000	8M	Extended FLASH 128 Kbytes	-	-
nCS4	0280:0000	8M	not used	-	-
Internal RAM	0300:0000	256k	Internal RAM 256k byte	32 bits	0
API RAM	FFD0:0000	4k	CPU/DSP shared RAM	16 bits	0
API Control	FFE0:0000	2k	CPU/DSP interface controller	16 bits	0
SIM	FFFE:0000	2k	SIM interface	16 bits	0
TSP	FFFE:0800	2k	Timed Serial Port	16 bits	0
TPU (REG)	FFFE:1000	1k	GSM time registers	16 bits	0
TPU (RAM)	FFFE:1400	1k	GSM timing unit	16 bits	0
RTC	FFFE:1800	2k	Real Time Clock	8 bits	0
ULPD	FFFE:2000	2k	Ultra Low-Power controller	16 bits	0
I2C	FFFE:2800	2k	I2C master serial	16 bits	0
SPI	FFFE:3000	2k	Serial port interface	16 bits	0
TIMER	FFFE:3800	2k	Software Timer 1	16 bits	0
UWIRE	FFFE:4000	2k	Synchronous Serial port	16 bits	0
ARMIO	FFFE:4800	2k	Keypad, buzzer, LCD & I/O	16 bits	0
TIMER2	FFFE:6800	2k	Software Timer 2	16 bits	0
LPG	FFFE:7800	2k	Light Pulse Generator	8 bits	0
PWL	FFFE:8000	2k	Pulse Width Light	8 bits	0
PWT	FFFE:8800	2k	Pulse Width Tones	8 bits	0
UART IRDA	FFFF:5000	2k	UART	8 bits	0
UART MODEM	FFFF:5800	2k	CPU/DSP shared RAM	8 bits	0
UART MODEM	FFFF:6000	2k	CPU/DSP interface controller	8 bits	0
RIF	FFFF:70000	2k	RF Interface	16 bits	0
WDT	FFFF:F800	256	Watchdog Timer	16 bits	0
INTH	FFFF:FA00	256	Interrupt Handler	16 bits	0
Memory IF	FFFF:FB00	256	Memory Interface	16 bits	0
DMA	FFFF:FC00	256	DMA Controller	16 bits	0
CLKM	FFFF:FD00	256	Clock Manager	16 bits	0

7.5. Interrupt Handler

The ARM CPU has two interrupts. FIQ is a Fast non-maskable interrupt and IRQ is a standard maskable interrupt.

HERCULES has 16 interrupt sources. The interrupt handler assigns priorities to these interrupts and routes them to either the FIQ or IRQ inputs of the ARM CPU. Additionally, the interrupt handler controls waking up of the CPU on receiving an unmasked interrupt, if the CPU is in sleep mode.

The FIQ interrupt is reserved for the power supply fail priority interrupt. This interrupt comes from OMEGA chip INT1.

Interrupt Level Assignments		
Interrupt Source	**Description**	**Interrupt detection**
IRQ0	Watchdog Timer INT	Edge sensitive
IRQ1	Timer 1 INT	Edge sensitive
IRQ2	Timer 2 INT	Edge sensitive
IRQ3	OMEGA fast interrupt	Low Level sensitive (FIQ)
IRQ4	TPU frame INT	Edge sensitive
IRQ5	TPU page INT	Edge sensitive
IRQ6	SIM INT	Edge sensitive
IRQ7	UART modem / IRDA INT	Low Level sensitive
IRQ8	Keyboard INT	Low Level sensitive
IRQ9	RTC periodical timer INT	Edge sensitive
IRQ10	RTC Alarm / ULPD / I2C INT	Low Level sensitive
IRQ11	ULPD gauge timer	Edge sensitive
IRQ12	External INT	Low Level sensitive
IRQ13	SPI INT	Edge sensitive
IRQ14	DMA INT	Low Level sensitive
IRQ15	API INT	Edge sensitive

The interrupt priorities are programmed through interrupt level registers. The interrupt has 23 registers:

$FFFF:FA00	Interrupt pending register	Read only / Reset
$FFFF:FA02	Mask interrupt register	Read / Write
$FFFF:FA04	IRQ source register	Read only
$FFFF:FA06	FIQ source register	Read only
$FFFF:FA08	IRQ source register (binary)	Read only
$FFFF:FA0A	FIQ source register (binary)	Read only
$FFFF:FA0C	Control Register	Read / Write
$FFFF:FA0E	IRQ0 interrupt register	Read / Write
	|	
$FFFF:FA2C	IRQ15 interrupt level register	Read / Write

7.6. General Purpose I/O

The general purpose I/O includes keypad scanning, two PWM ports and 16 general purpose I/O lines. The I/O lines are multiplexed onto other functions - if one I/O is selected, the other function is unavailable.

I/O Pin Assignments					
Signal		Pin	Function	Description	I/O
I/O (0)	TPU_WAIT	28	Model status 0 (LSB)	11: GD93	
I/O (1)	TPU IDLE	30	Model status 1 (MSB)		
I/O (2)	IRQ4	50	Battery_ID	L = Ni-MH H = Li+	
I/O (3)	SIM RnW	59	LCD_RS	H = Data L = Command	
I/O (4)	TSP_DI	130	VSRFEN	H = RF common power enable L = FR common power disable	
I/O (5)	SIMPWRCTL	105	used for pull-up resistor		
I/O (6)	BCLK_X	117	VIB_ON	H = Vibrate ON L = Vibrate OFF	
I/O (7)	nRESETOUT	100	NRESETOUT		
I/O (8)	MCUEN	159	BackCaseLight	H = LED_ON L = LED_OFF	
I/O (9)	MCSI_TXD	150	MCSI_TXD	DAI Tx Data	
I/O (10)	MCSI_RXD	151	MCSI_RXD	DAI Rx Data	
I/O (11)	MCSI_CLK	152	MCSI_CLK	DAI Clock	
I/O (12)	MCSI_FSYNCH	154	MCSI_FSYNCH	DAI Frame synchronisation	
I/O (13)	MCU_EN(2)	56	CHARGE_LED	H = Charge LED ON L = Charge LED OFF	
I/O (14)	nBHE	50	nBHE		
I/O (15)	nBLE	48	nBLE		

7.7. Dedicated I/O

Dedicated I/O lines are reserved for the back-light, ringing tone and keyboard.

The loudness of the tone is controlled by a PWM (Pulse Width Modulation) and melody volume control signals.

LED brightness is controlled by PWL (Pulse With Light modulation). Lighting interval is also controlled by LPG (LED Pulse Generator). Adjustment of LED brightness is not supported and, thus, the LT function is used to set maximum level (3Fh).

The PWM are outputs only.

PWM Pin Assignments			
Signal	Pin No.	Function	I/O
PWL	4	LED control	-
PWT/ BU	2	Buzzer (6-bit PWM)	O

The PWM(BU) is clocked at 13/3MHz.

Tones are generated by using timer 1 to switch the buzzer PWM on and off at the frequency of timer 1. Ringing tones can be played by altering the value of timer 1. During melody ringer operation, two output signals are controlled for clarity.

During Handsfree operation, the ringing tone is derived from the DSP tone generator.

8 OMEGA

8.1. Introduction

Omega contains the interface circuits to the Audio, RF and auxiliary functions for the baseband circuit.

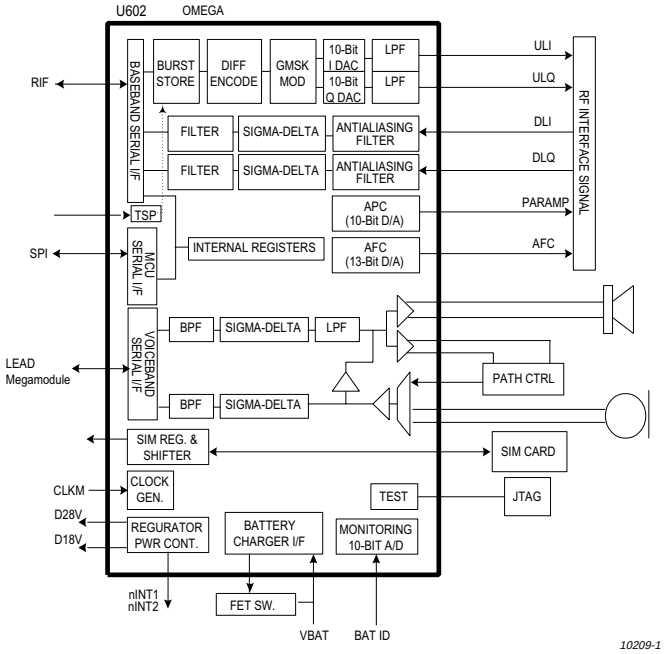

Figure 8.1: Omega Block Diagram

8.2. Uplink I and Q

Omega performs GMSK modulation on Data samples received from HERCULES at 270 bits per second.

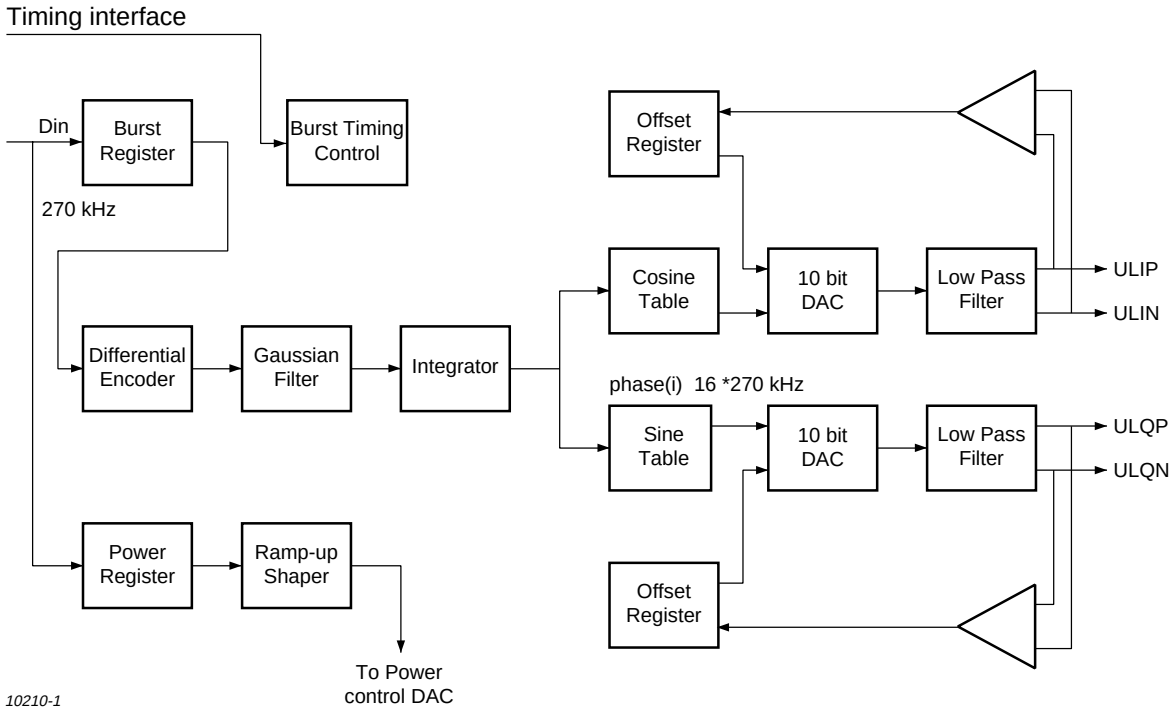

Figure 8.2: Functional structure of the baseband uplink path

8.3. Downlink I and Q

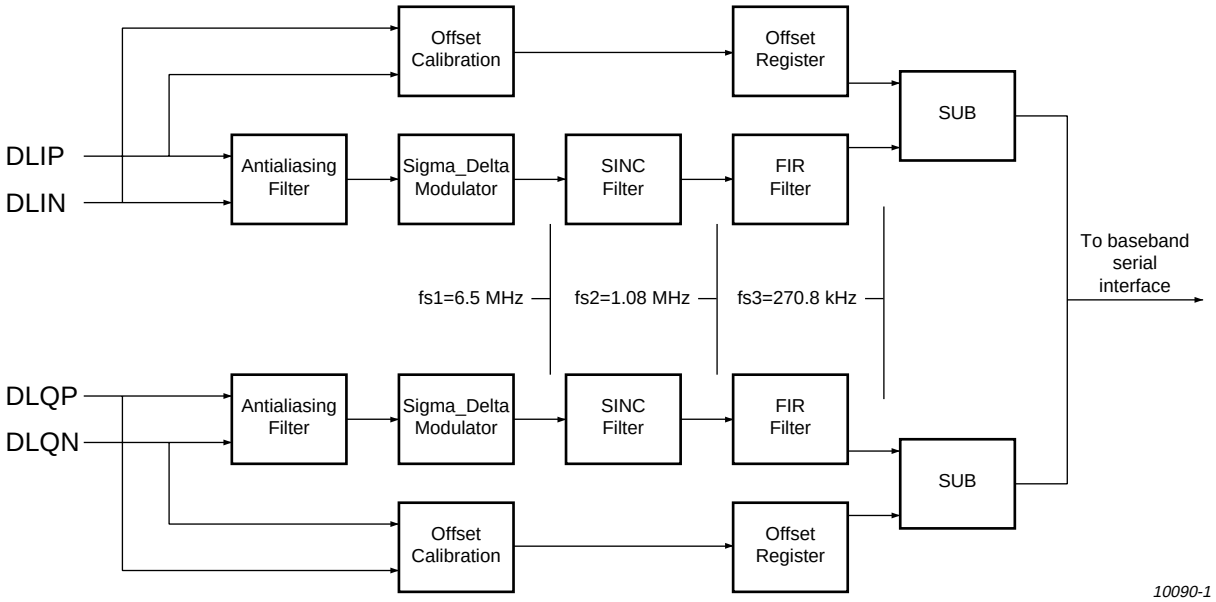

Figure 8.3: Function structure of the baseband downlink path

8.4. Power Amplifier Ramp

The PA Ramp is formed by two D/A. The first, a 5-bit D/A, defines the ramp shape; the second, an 8-bit D/A, defines the maximum level.

The ramp shape is defined by 64 steps. The shape can be defined differently for rising and falling ramps. Typically, a raised cosine shape will be used as a starting basis of the ramp shape.

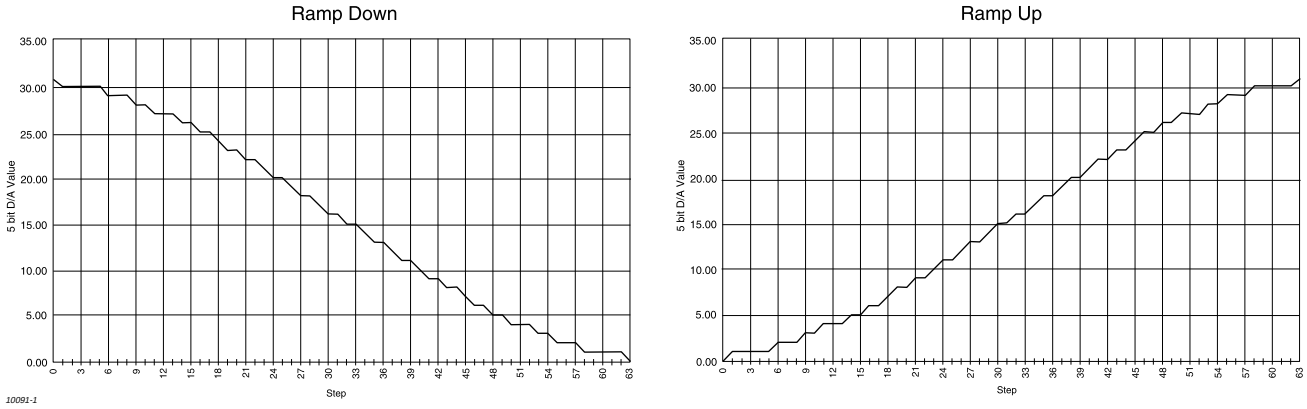

Figure 8.4: Example for the PA ramp

The raised cosine shape will be modified to compensate for RF circuit characteristics.

The ramp time is selectable between each step being 1/16 of a bit and being 1/8 of a bit, giving a maximum ramp time of either 14.77 μs or 29.53μs.

An 8-bit value is used to program the ramp output level.

8.5. AFC Control

The 13 MHz system clock frequency is controlled by a 13-bit sigma-delta D/A in the OMEGA chip.

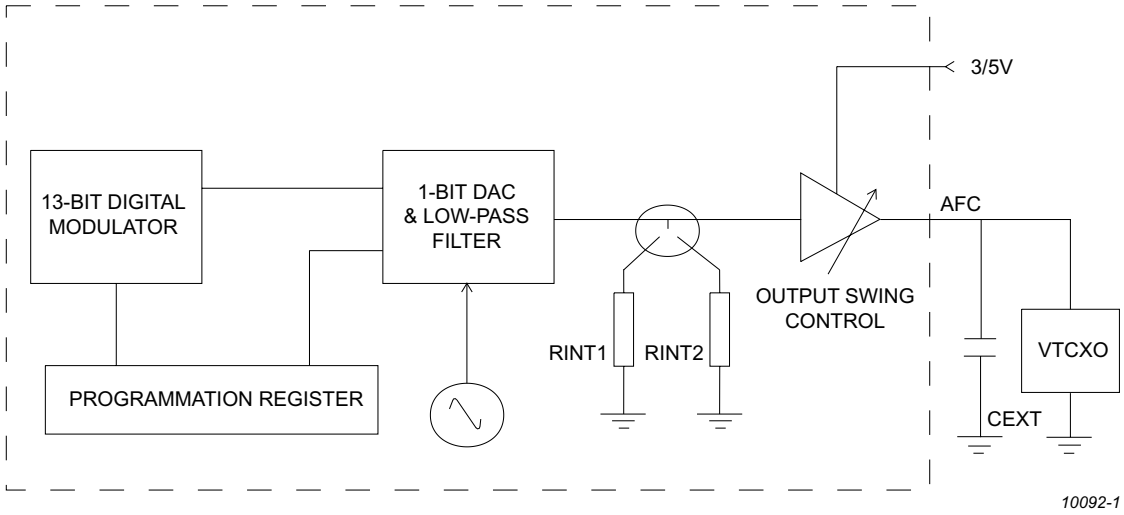

Figure 8.5: AFC Block Diagram

8.6. Audio

OMEGA provides the analogue interface for the digital audio samples processed by the DSP in HERCULES.

8.6.1. Voice Uplink Path

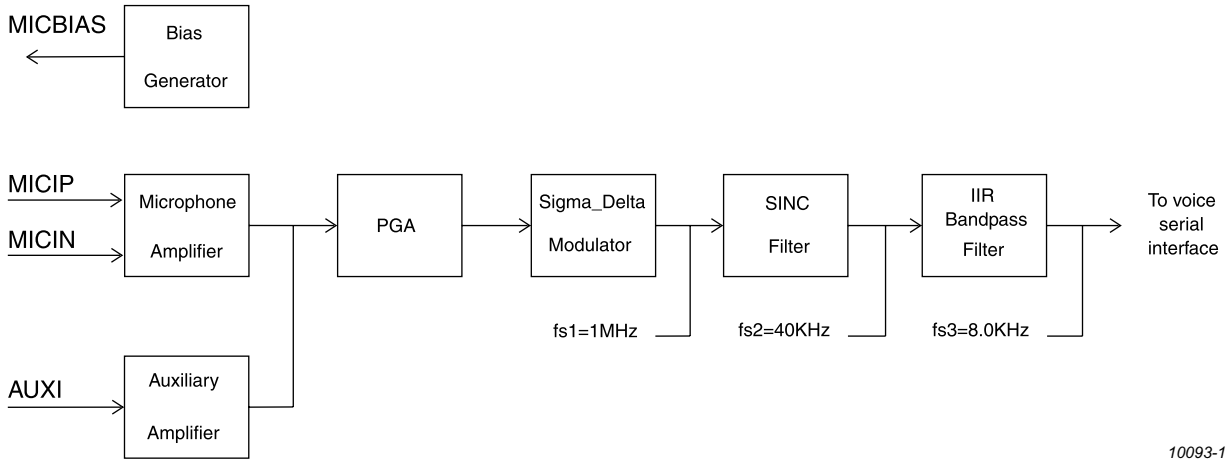

Figure 8.6: Voice ADC Block Diagram - Uplink Path

8.6.2. Voice Downlink Path

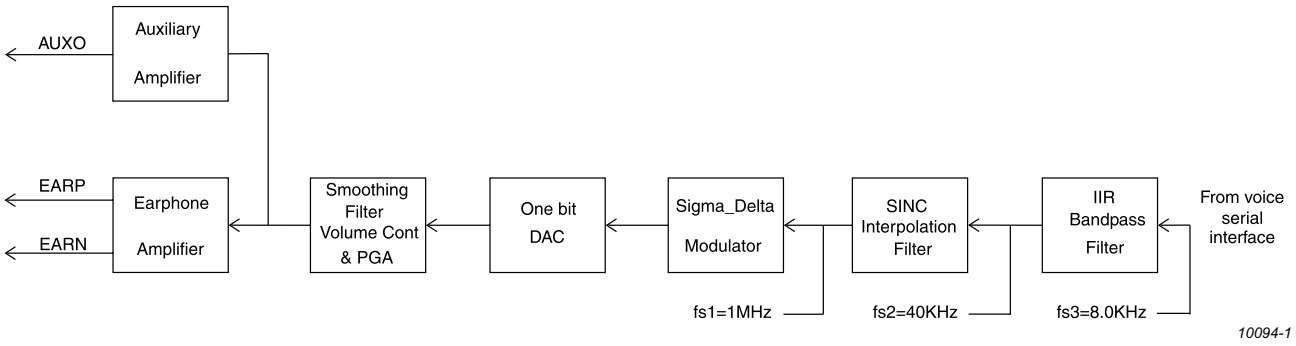

Figure 8.7: Voice ADC Block Diagram - Downlink Path

8.7. Auxiliary A/D

OMEGA provides five 10-bit A/D converter inputs for monitoring purposes as follows:

OMEGA A/D Inputs			
OMEGA Input	**Pin No.**	**Function**	**Values**
ADIN1	90	NC	
ADIN2	89	Battery Temperature	54 = +70 °C 208 = +25 °C 700 = -20 °C 1000 = No Battery
ADIN3	88	N/C	
ADIN4	87	N/C	
ADIN5	86	N/C	

8.8. Charging Voltage Control

OMEGA provides 10 bits for AGC control. As Rx gain is not controlled by DAC, it is used for charging control. The DAC output is able to control accurately the charging for Li+ and NiMH batteries. The telephone has electrical volume for calibration of this DAC.

9 POWER SUPPLIES

9.1. Introduction

This section describes the Power Supply Unit (PSU) used on the Main PCB and the method by which it is controlled. The Battery life during GSM 1800 operation benefits from lower transmit power and higher PA efficiency and is therefore more efficient than when operating in GSM 900.

This section has detailed information on:

1. An overview of the circuit functionality.
2. Powering-up the phone.
3. Powering-down the phone.
4. Power management.

9.2. Overview

The logic circuit uses three separate power supplies as follows:

1. 2.8 Volts supply is used for the main power supply, 2V8 provides power to the digital part of the baseband circuit (HERCULES, Memory and LCD). A2V8 is used to power the analogue part of the baseband circuit (OMEGA and voice memo).
2. 1.8 Volts is provided to power internal blocks within the HERCULES (ARM, DSP, ASIC).
3. 5.0 Volts (SIM_PWR) is provided to power the SIM and the SIM interface. This is enabled only when it is necessary to communicate with the SIM.

The RF circuit uses three power supplies each provided by a separate 2.8 Volt regulator within U401. They are:

- VSRF and VS_VCO which are present when the LO_EN signal is present.
- VS_RF and VS_VXCO which are present when the signal RF_ON is present.

The power amplifiers are powered directly from the battery VBAT.

9.3. Power-up

9.3.1. Power Modes

The power-up procedure has two phases. If an initial check to see if the battery is in good condition is successful, the second phase determines the source of the power-up request, key press, external power, accessory, etc. and acts accordingly.

The phone can be defined as powered-on whenever the linear regulators are active. It is not always obvious to the user that the phone is powered-on as it may be in one of four modes

Mode	Description
Sleep	In this mode the CPU has been prevented from deactivating the linear regulators by EXT_PWR. There is no CPU activity.
Charge	The CPU is alive but may perform only battery charging functions and monitor the power key.
Restricted	LEDs light, beeps, can charge battery etc. but it is not permitted to use the radio.
Active	The mobile is fully functional; LEDs light, beeps, search for network etc.

9.3.2. Battery Condition

The CPU must check the battery condition before deciding to power-up. The CPU can measure battery voltage and temperature. If the battery temperature measurement is invalid, a non-standard battery has been fitted, the battery is missing or the whole phone is operating far outside its specified temperature range, the phone is not powered-up. The CPU will regularly monitor the battery condition while the phone is on.

If EXT_PWR is present, the regulators will be forced on and the CPU will be unable to deactivate them. If the CPU wants to power-down, all it can do is to enter sleep mode.

Battery Voltage (V)	Temp Reading	EXT_PWR	Result
X (don't care)	invalid	<VBAT + 0.4 V	Power-down (battery fault)
X	invalid	>VBAT + 0.4 V	Sleep (battery fault)
<3.0	X	<VBAT + 0.4 V	Power-down (low battery)
<3.5	valid	<VBAT + 0.4 V	LOW
>3.5	valid	X	OK

9.3.3. Power-up Sequence

The power-up sequence can be initiated by pressing the power key, or by applying a power source to the EXT_PWR signal line. Both enable the linear regulators and the CPU becomes active. The CPU must then check the battery condition; if the phone is not required to power-down or sleep immediately, the result must be OK or LOW. The CPU then checks to see if a hands-free unit is connected by polling the nACC_SENSE signal, LOW when HF is connected.

Now the CPU can determine whether to remain powered-up or not, according to the truth-table shown below. In each case the active parameters are shaded.

Battery Condition	EXT_PWR	nACC_SENSE	KBR0	ACC_PWR	Mode
OK	X	X	1	1	active
LOW	>VBAT + 0.4 V	X	1	1	restricted
OK or LOW	>VBAT + 0.4 V	X	0	1	charge
OK	>VBAT + 0.4 V	<0.5 V	0	1	active or charge
LOW	>VBAT + 0.4 V	<0.5 V	0	1	restricted or charge

With a hands-free unit connected, the phone can be configured via the MMI to power-up and down with transitions of the vehicle ignition. These are sensed by the CPU on nACC_SENSE.

Any other state than those in the table will cause the phone to deactivate the PSU by setting STAY_ALIVE LOW.

While the CPU is active, it must monitor the battery condition and accessory connectivity and change state accordingly.

Current Mode	EXT_PWR	nACC_SENSE	KBR0	Battery Condition	New Mode
Charge	X	X	1	OK	active
Charge	>VBAT + 0.4 V	X	1	LOW	restricted
Restricted	X	X	0	OK	active

9.4. Power-down

There are two power-down procedures:

Procedure	Description
Normal power-down	In this case, the software has full control over the power-down procedure. Calls can be terminated gracefully etc. In some cases the PSU is not deactivated but there is a change of operating mode.
Emergency power-down	This situation is caused by battery removal and is flagged by FIQ. In this case, the CPU only has time to perform a subset of the normal procedure. The priority is to prevent corruption of SIM data.

The truth-table for the power state transitions is shown below. In some cases the phone does not power-down completely but may enter a state of reduced functionality, e.g. from active to charge mode.

Current mode	Battery Voltage	HF	nACC_SENSE	FIQ	KBR0	EXT_PWR	power-down	New mode
X		X	X	1	X	< VBAT + 0.4 V	normal	OFF
X	X	X	X	0	X	X	emergency	OFF
X	X	X	X	1	1	< VBAT + 0.4 V	normal	OFF
active	<3.4 V	X	X	1	0	> VBAT + 0.4 V	normal	restricted
active	<3.5 V	no	X	1	1	> VBAT + 0.4 V	normal	charge
active	<3.4 V	yes	>2.5 V	1	1	X	normal	OFF
active	<3.4 V	yes	<0.5 V	1	1	> VBAT + 0.4 V	normal	charge
active	<3.4 V	yes	>2.5 V	1	0	X	normal	OFF
active	X	no	X	1	1	> VBAT + 0.4 V	normal	charge
active	X	yes	<0.5 V	1	1	> VBAT + 0.4 V	normal	charge
active	X	yes	>2.5 V	1	1	X	normal	OFF
active	X	yes	>2.5 V	1	0	> VBAT + 0.4 V	normal	OFF
active	X	X	X	1	0	< VBAT + 0.4 V	normal	OFF

9.5. Power Management

9.5.1. Overview

The power supply circuit supplies regulated power to the base-band parts, controls battery charging and monitors battery usage.

The Power Management section consists of five parts as follows:

1. Power Source.
2. Power On/Off Control & Power Source Failure.
3. Voltage Regulation.
4. Battery Charging & Monitoring.
5. Accessory Control.

The power amplifiers are powered directly from the battery supply to maximise the power available to them. They operate at full specification between 3.0 and 3.6 Volts.

9.5.2. Power Source

EB-BSD93 battery packs use Lithium-Ion cells which have the advantage of reduced weight, size and improved gravimetric and volumetric densities compared to that of Ni-MH cells.

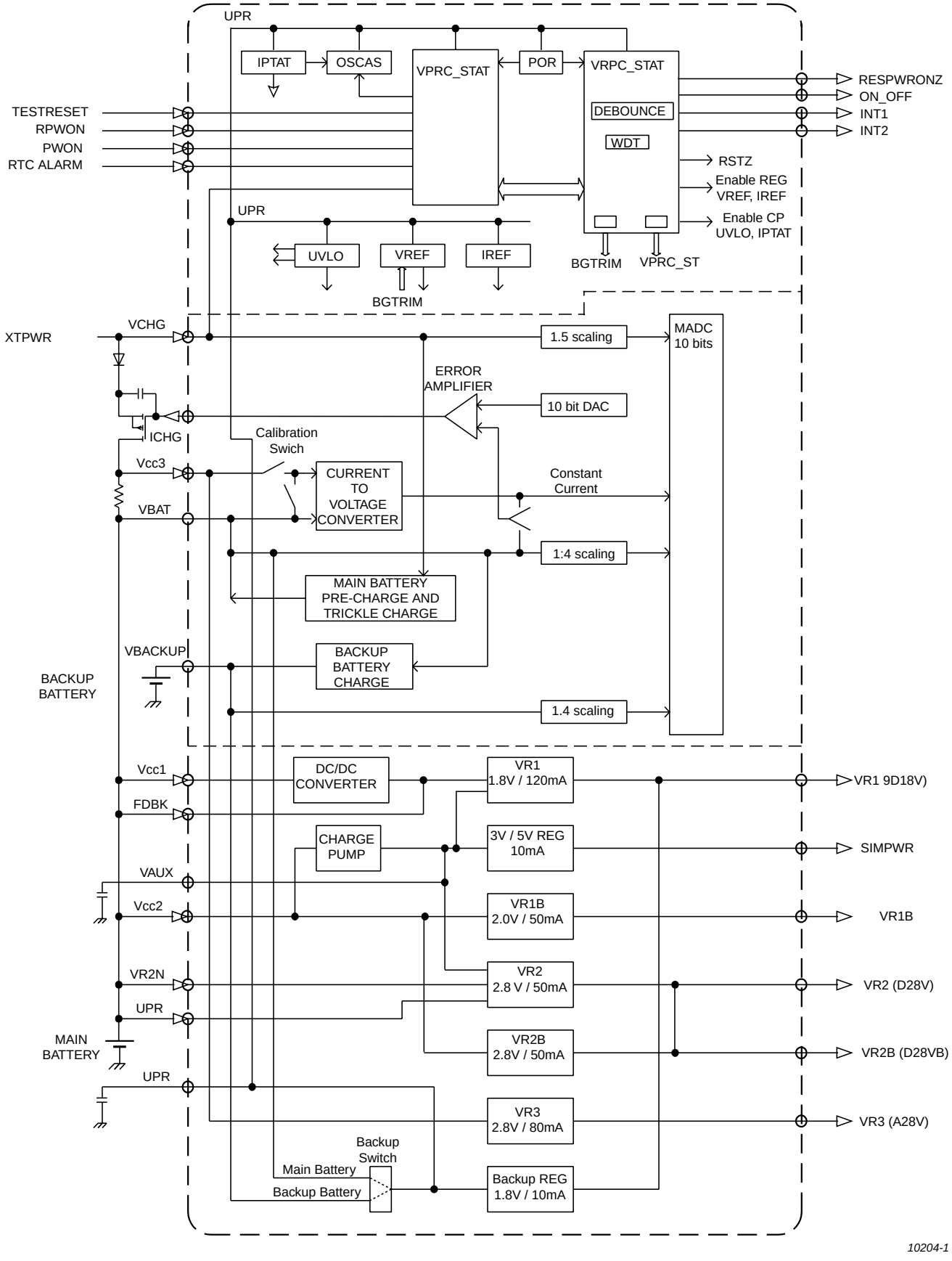

Figure 9.1: Power Supply Block Diagram

9.5.3. Power On-Off Control

The hardware model for the Power On/Off Control and Power Source Failure functions can be expressed by the following boolean expression and logic diagram.

On/Off = $\overline{VBAT}$ + ((nPOWKEY · $\overline{RTC\_INT}$ · $\overline{EXT\_PWR}$) + n$\overline{LVA_INT}$)

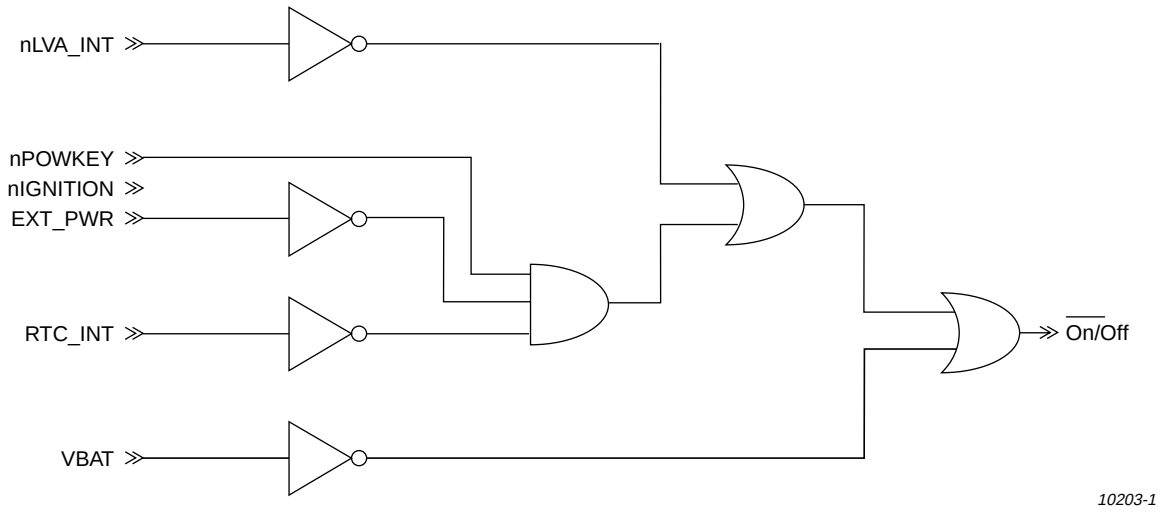

Figure 9.2: Power On / Off Control and Power Source Failure Logic Diagram

On/Off: Initially this active low signal is under Hardware control, the purposes of which are as follows:

1. Enable all voltage supplies to OMEGA (D28V, D28VB, A28V, D18VB & D18V).
2. Enable VSRF & VSVCXO voltage supplies to RF.
3. Generation of OSCAS Master Clock signal.
4. Set nRESET signal LOW.
5. Wait approximately 200 ms for the voltage output of the regulators and 13 MHz Clock to become stable. Allow reset of HERCULES and OMEGA internal blocks.
6. Set nRESET HIGH causing the ARM processor to start from address 0.

9.5.4. Power Source Failure

The SIM card contains EEPROM. If the battery power fails while the SIM is active, the SIM may corrupt its memory as the power supply drops out of specification.

The FIQ(nLVA) is a non-maskable interrupt generated by OMEGA and sent to the CPU which forces exception processing whenever the main battery voltage drops below 2.7 V.

9.5.5. Voltage Regulation

The telephone has the following power sources:

DV28V: Baseband power supply for digital and analogue circuitry:

Voltage:	2.9 V ±0.2 V
Current:	120 mA max.
Dropout:	150 mV max (max. load)

Provides the main power for the baseband digital part (Hercules, memories and LCD) and some analogue circuits.

DV28VB: Power Supply for Hercules ASIC I/O

Voltage: 2.9 V ±0.2 V
Current: 120 mA max.
Dropout: 150 mV max (max. load)

Provides power for the ASIC I/Os in Hercules.

D18V: Power Supply for Hercules LMM block

Voltage: 1.8 V ±0.15 V
Current: 120 mA max.
Dropout: 250 mV max (load max)

Provides power for the HERCULES Lead Mega Module block

D20V: Digital Power Supply for Omega

Voltage: 2.0 V ±0.2 V
Current: 50 mA max.
Dropout: 500 mV max (load max)

Provides power for the OMEGA internal analogue circuits.

VBB: Voltage for Hercules Core Block backup

Voltage: 1.6 V ±5 %
Current: 120 mA max.
Dropout: 150 mV max (load max)

Power provided by the backup battery to maintain HERCULES internal memory.

9.5.6. Battery Charging and Monitoring

The status of the LCD battery icon is determined by the value of 'BAT_VOLT' returned from OMEGA as shown in the following table:

Icon Status	Battery Pack	
3 bar	3.77 V	
2 bar	3.68 V <	< 3.77 V
1 bar	3.46 V <	< 3.68 V
Low Voltage Alarm		< 3.46 V

Battery charging is controlled by the CPU. If rechargeable cells and external power are detected and the temperature is within specified limits, the rapid charge algorithm is started.

Charging is determined by constant voltage and constant current control with time, temperature and voltage safeguards. A current limit no greater than the maximum charge current for any battery option must be provided by the external power source.

Deeply discharged batteries may not have enough power to initiate charging. In this case, the charging circuit must automatically start trickle charging until there is enough power to switch on the telephone.

9.5.7. Accessory Control

The telephone can detect accessories connected to the I/O connector and control the power supply to them. These are controlled by the signal lines detailed in the following table.

Note that the software needs to set ACC_PWR high before checking DATA_MODE0 and DATA_MODE1.

Inputs (Pin No.)				Outputs	Peripherals
DATA_ MODE0 (4)	**DATA_ MODE(10)**	**nACC_SENSE (5)**	**EXT_PWR (13)**	**ACC_PWR (9)**	
High	High	High	Low	Low	none
High	High	High	High	Low	AC / DC
Low	Low	Low	Low	High	SMS cable
Low	High	Low	Low	High	DA
High	Low	Low	Low	High	Soft Modem Bluetooth Adaptor
High	High	Low	High	High	H/F
High	High	Low	Low	High	(H/F)
Low	Low	Low	High	High	H/F, SMS cable
Low	Low	Low	Low	High	(H/F), SMS cable
Low	High	Low	High	High	H/F, DA
Low	High	Low	Low	High	(H/F), DA
High	Low	Low	High	High	H/F, Software Modem Bluetooth Adaptor
High	Low	Low	Low	High	(H/F), Software Modem Bluetooth Adaptor
High	High	Low	Low	High	Test Jig

Any data accessories connected to the Car Kit without a power supply behave as if they were connected directly to the handset. Input status in this case is as without Car Kit connected.

KEY:

H/F	Car kit with Handsfree operation (either full or basic operation)
(H/F)	Car kit is connected without power supply (handheld operation)
AC/DC	AC Adaptor, DC Adaptor
DA	PCMCIA card data adaptor
SMS	SMS / Software modem cable

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