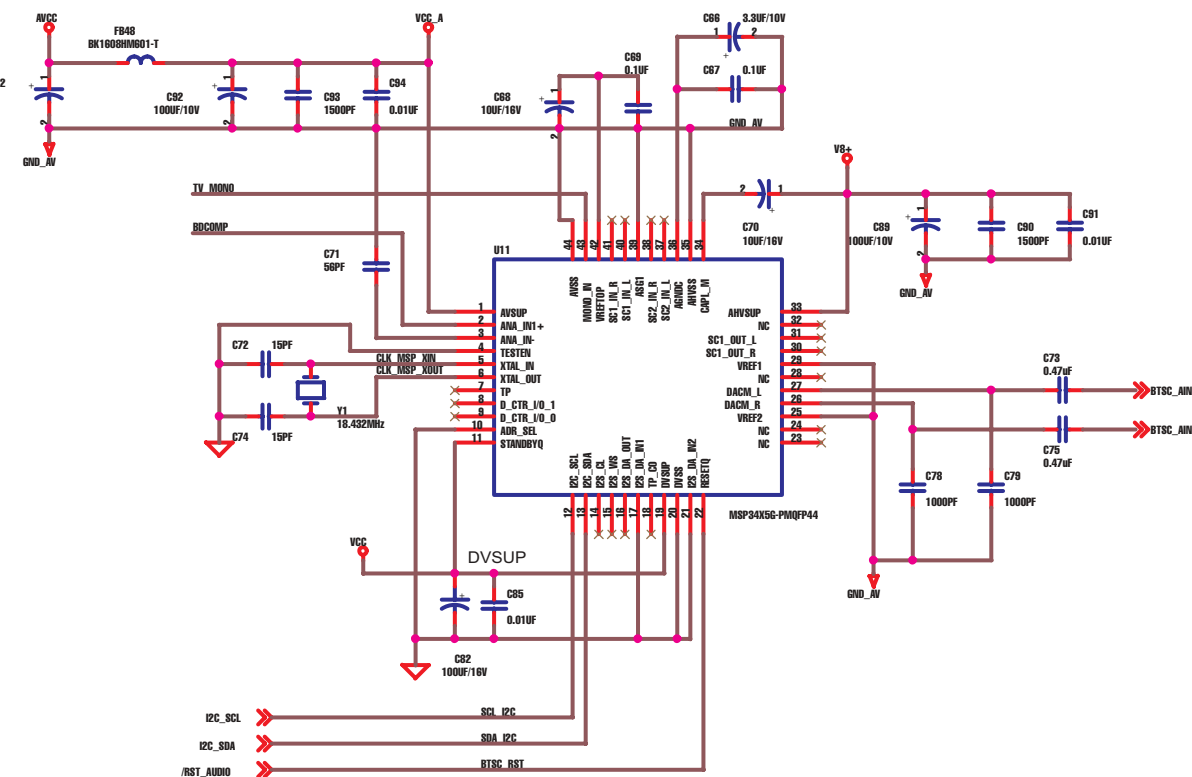
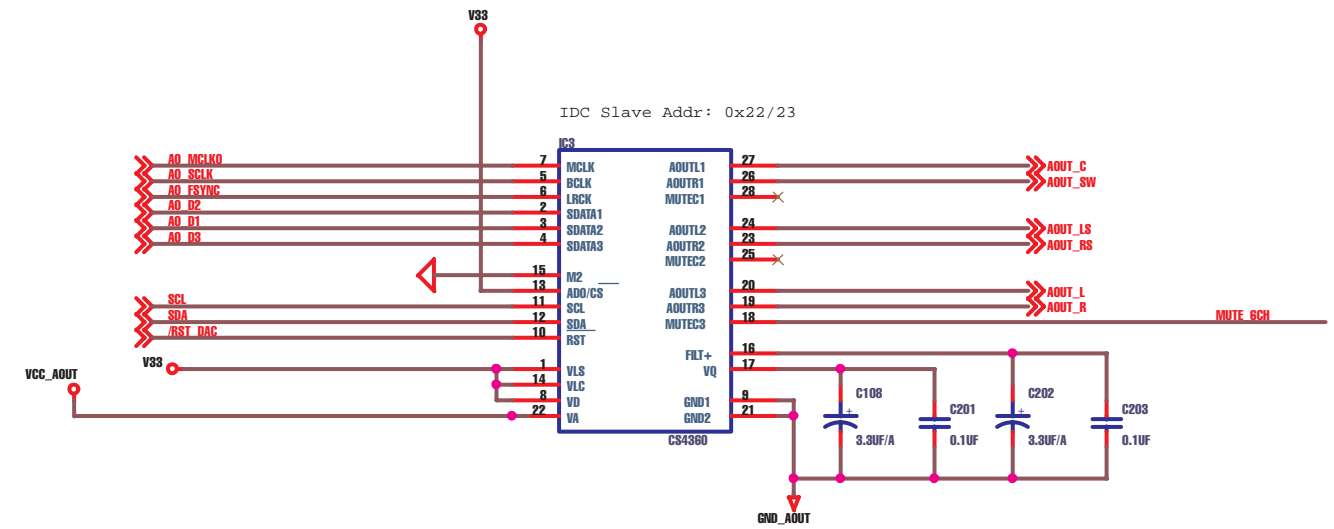
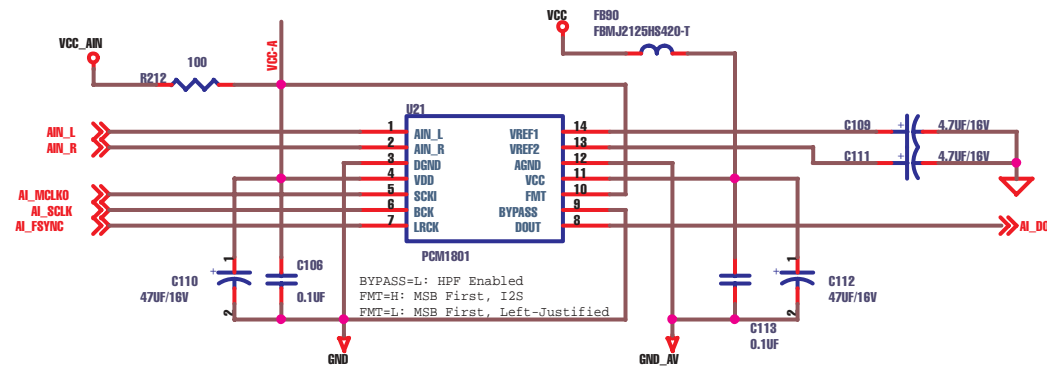


BTSC
 IDC Slave Addr: 0x80/81
 USA: MSP3425G
 EURO: MSP3415G

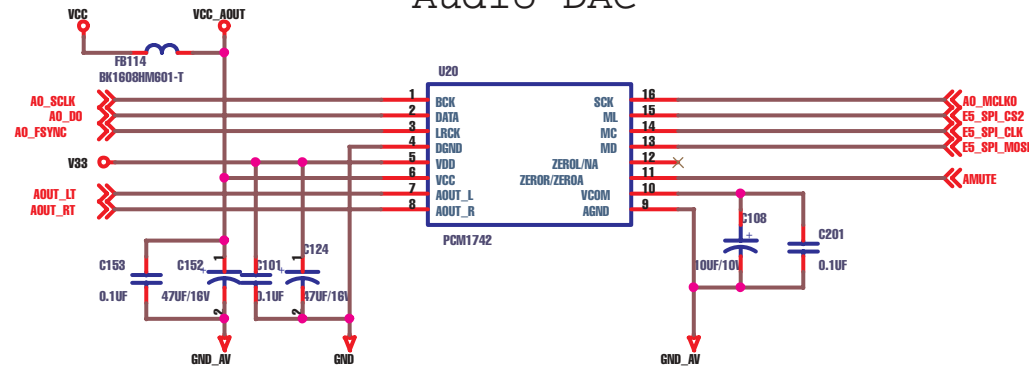


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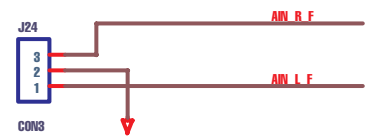
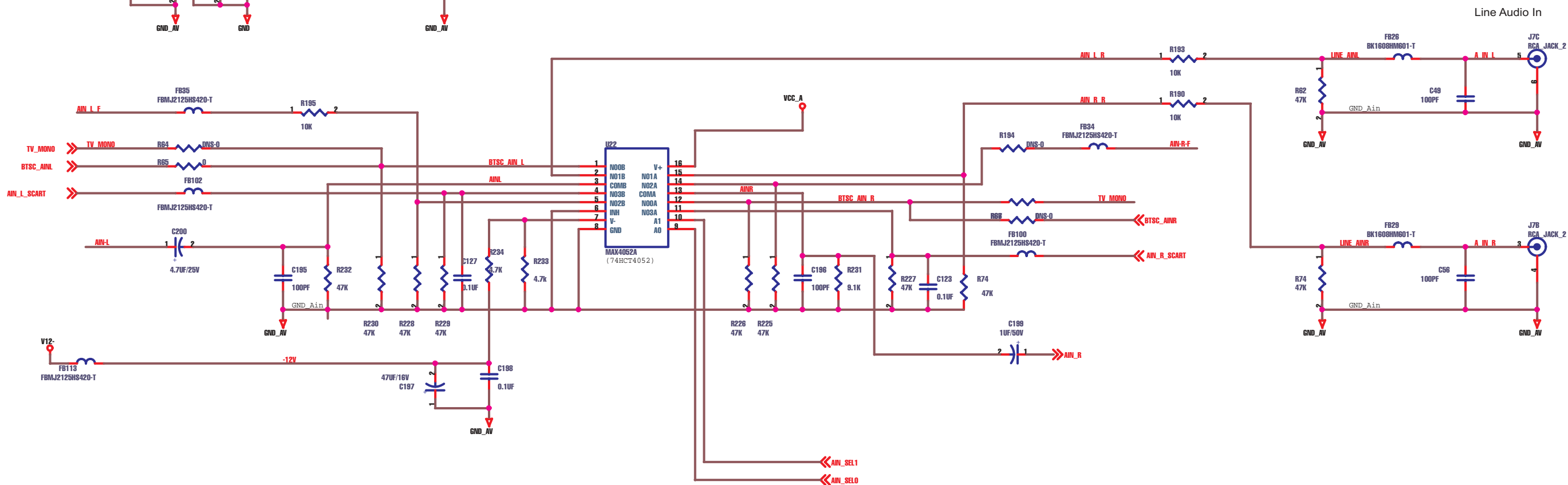
Audio ADC



Audio DAC



Line Audio In

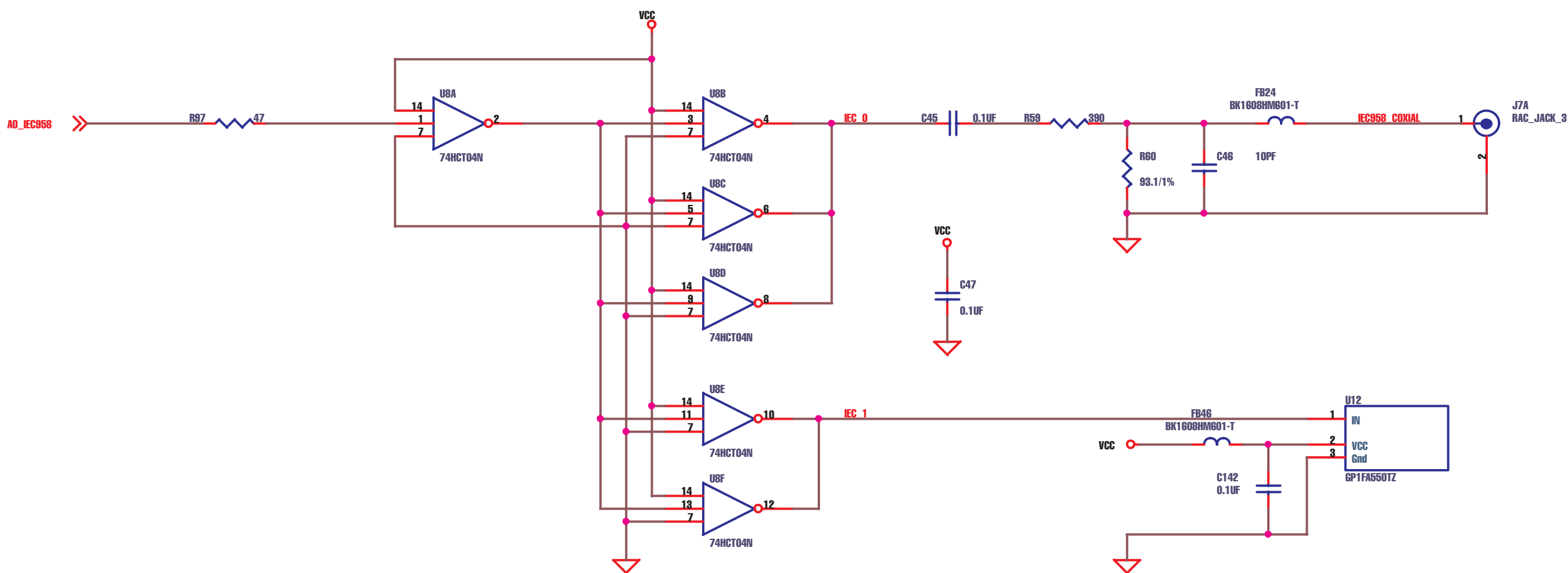


Front Line Audio In

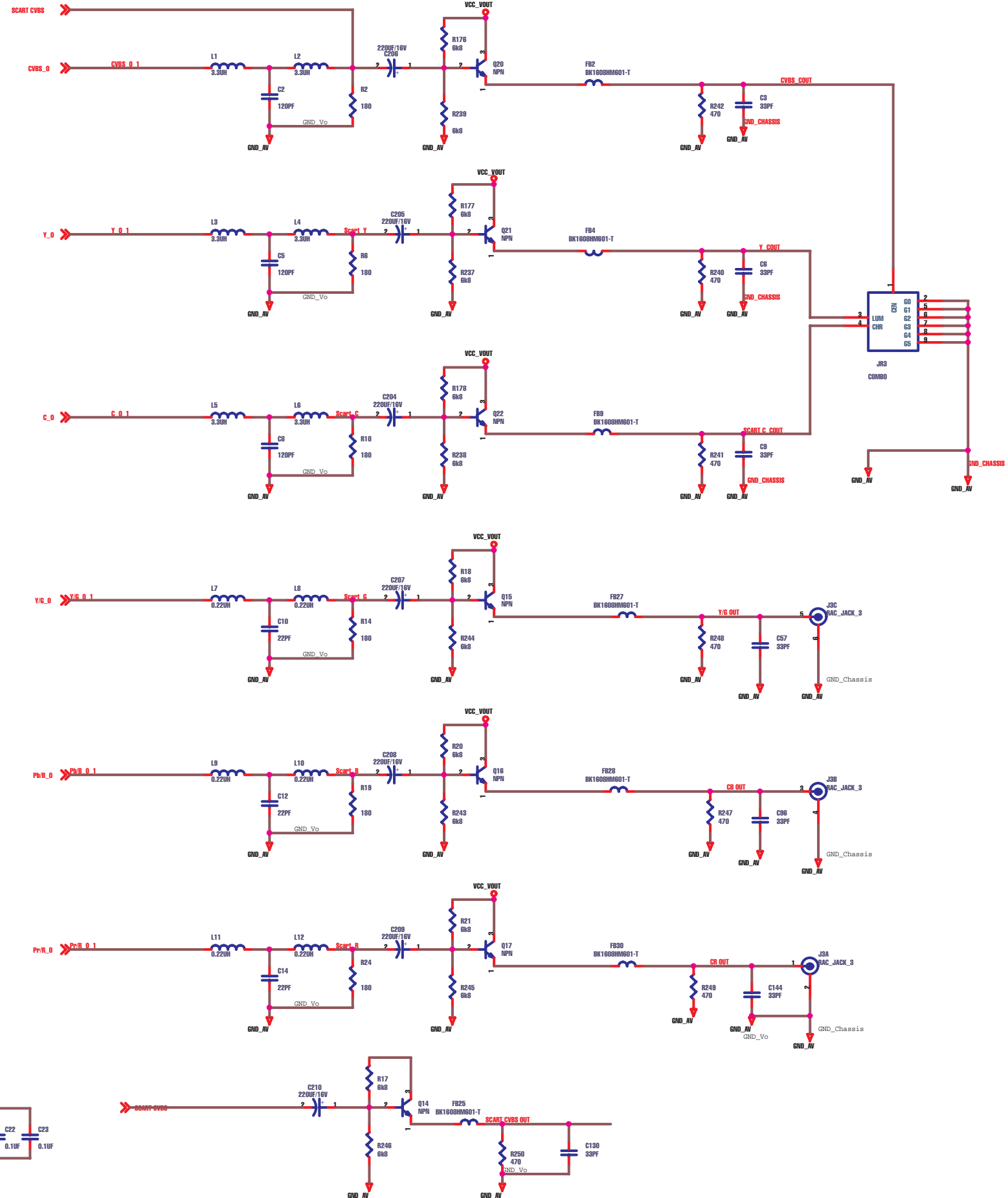
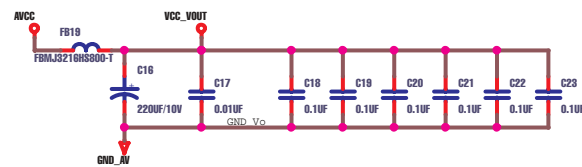
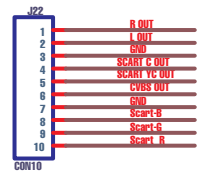
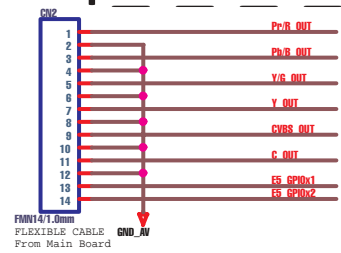
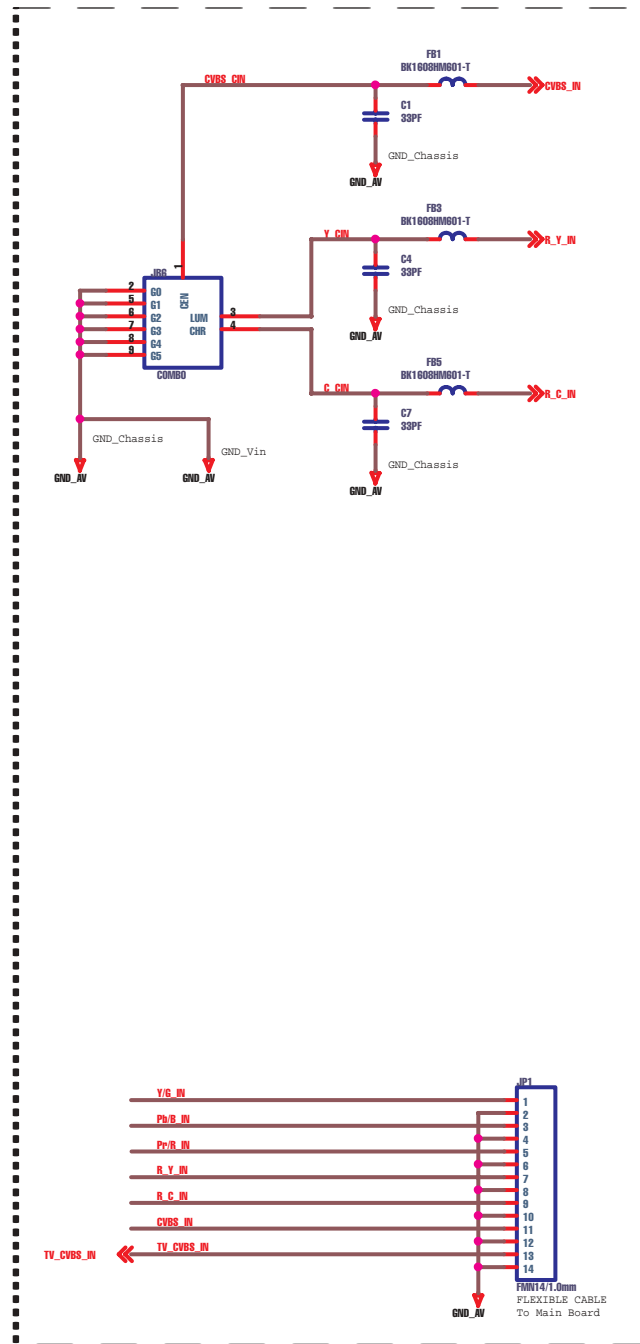
AIN_SEL[1:0]	Audio Source
00	BTSC/TUNER
01	Audio In(Back)
10	Audio In(Front)
11	SCART in

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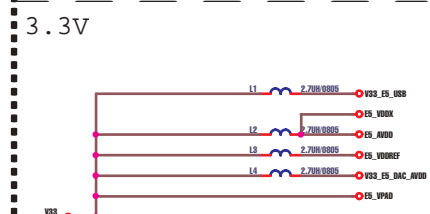
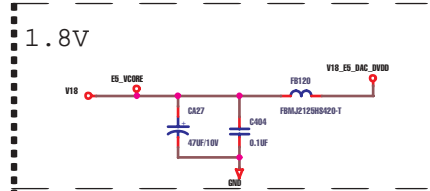
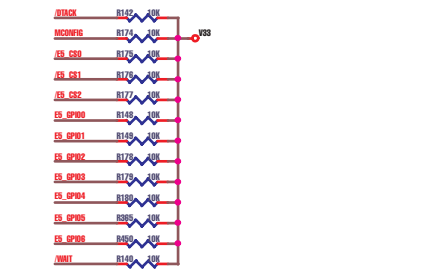
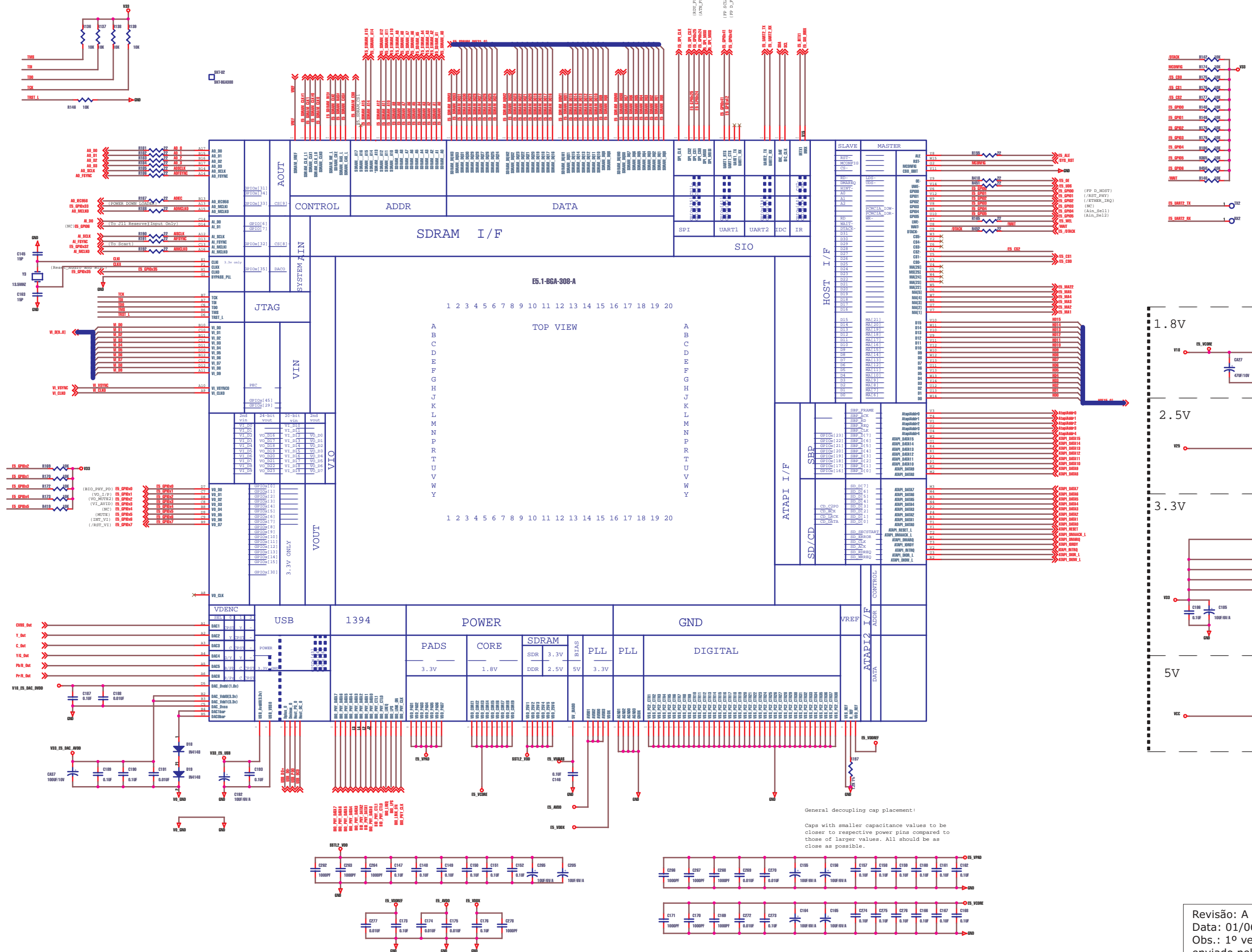
Digital Audio Out



ESQUEMA ELÉTRICO - DR-660

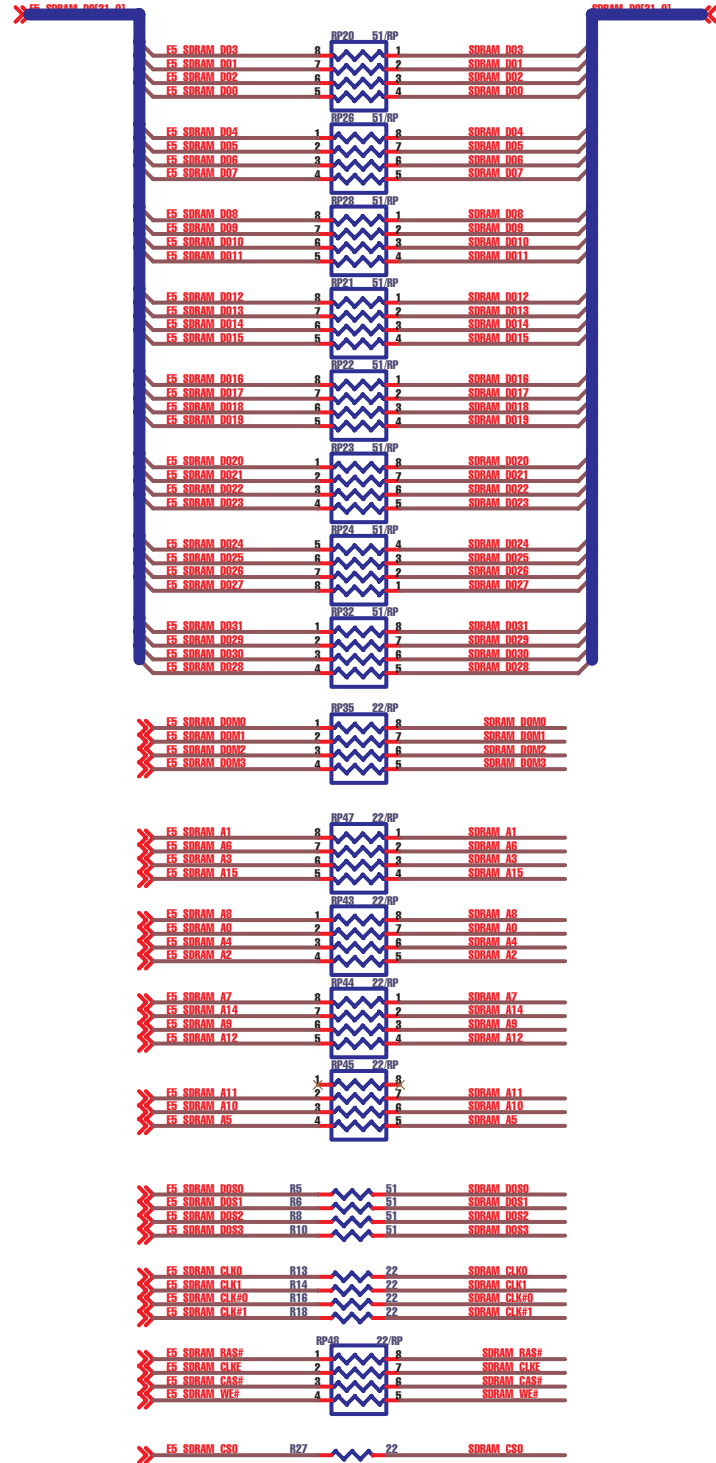


Revisão: A
 Data: 01/06/05
 Obs.: 1º versão do Esquema elétrico enviado pelo fornecedor

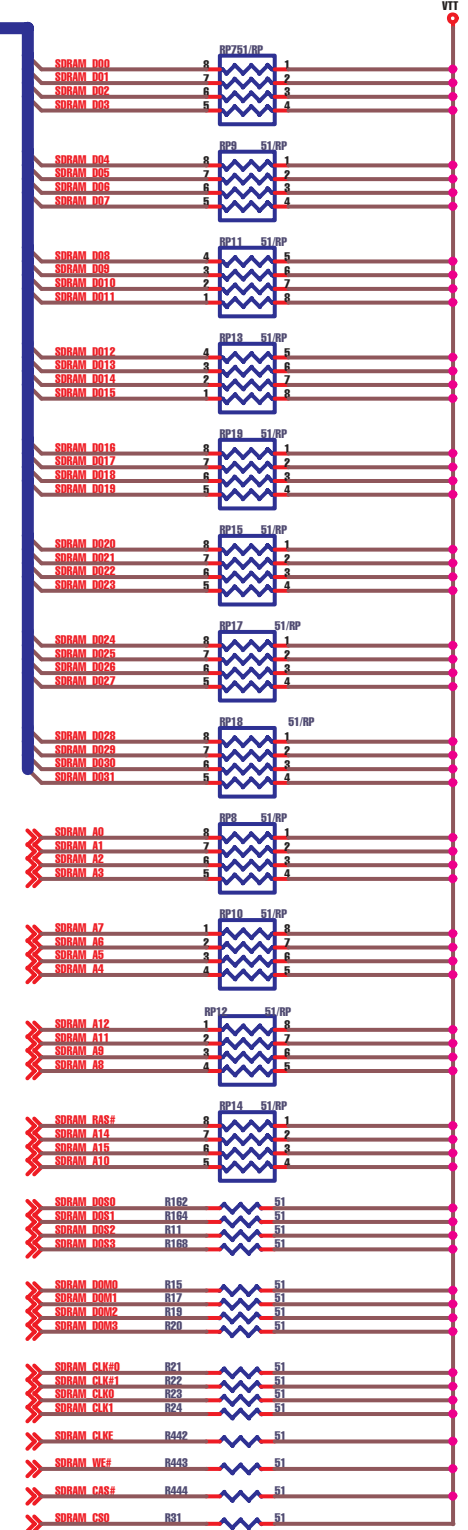
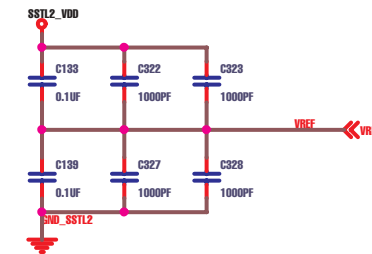
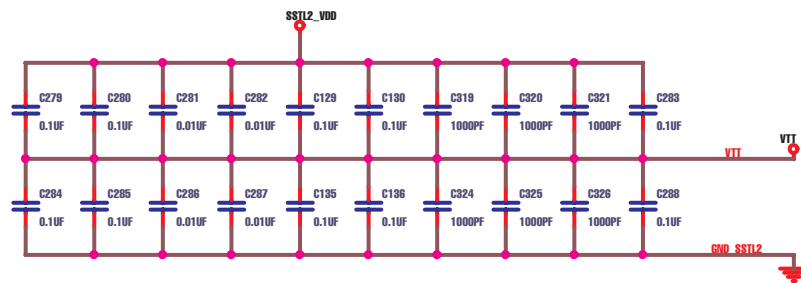
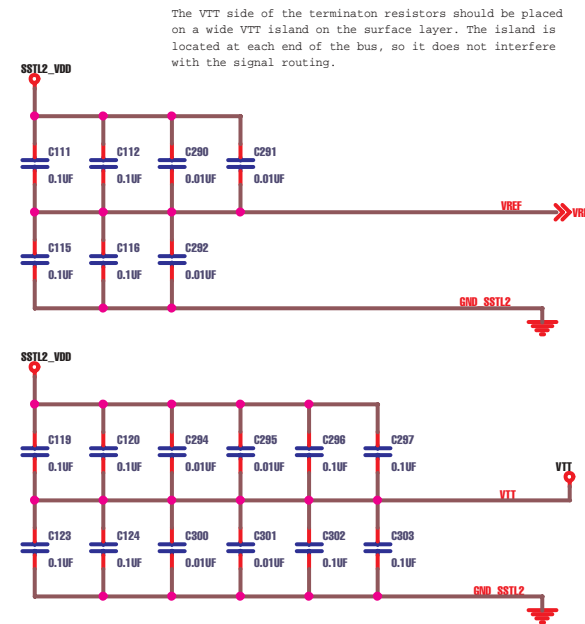


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TERMINATION AT E5.1



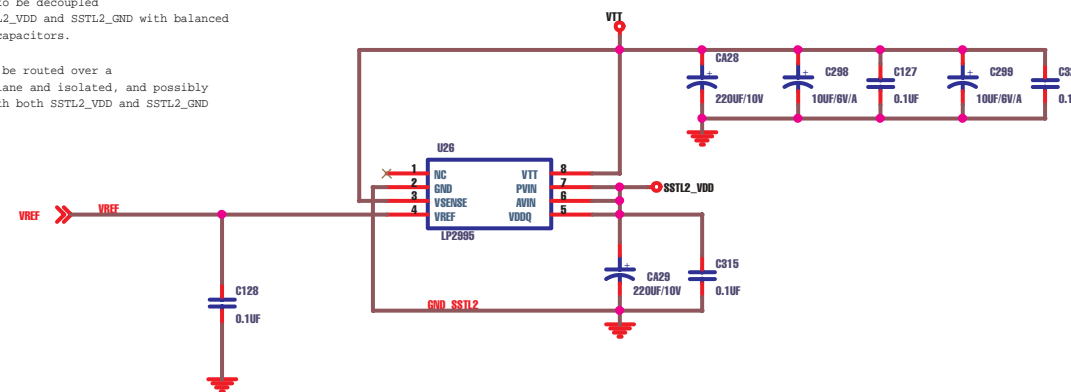
TERMINATION AT DDR

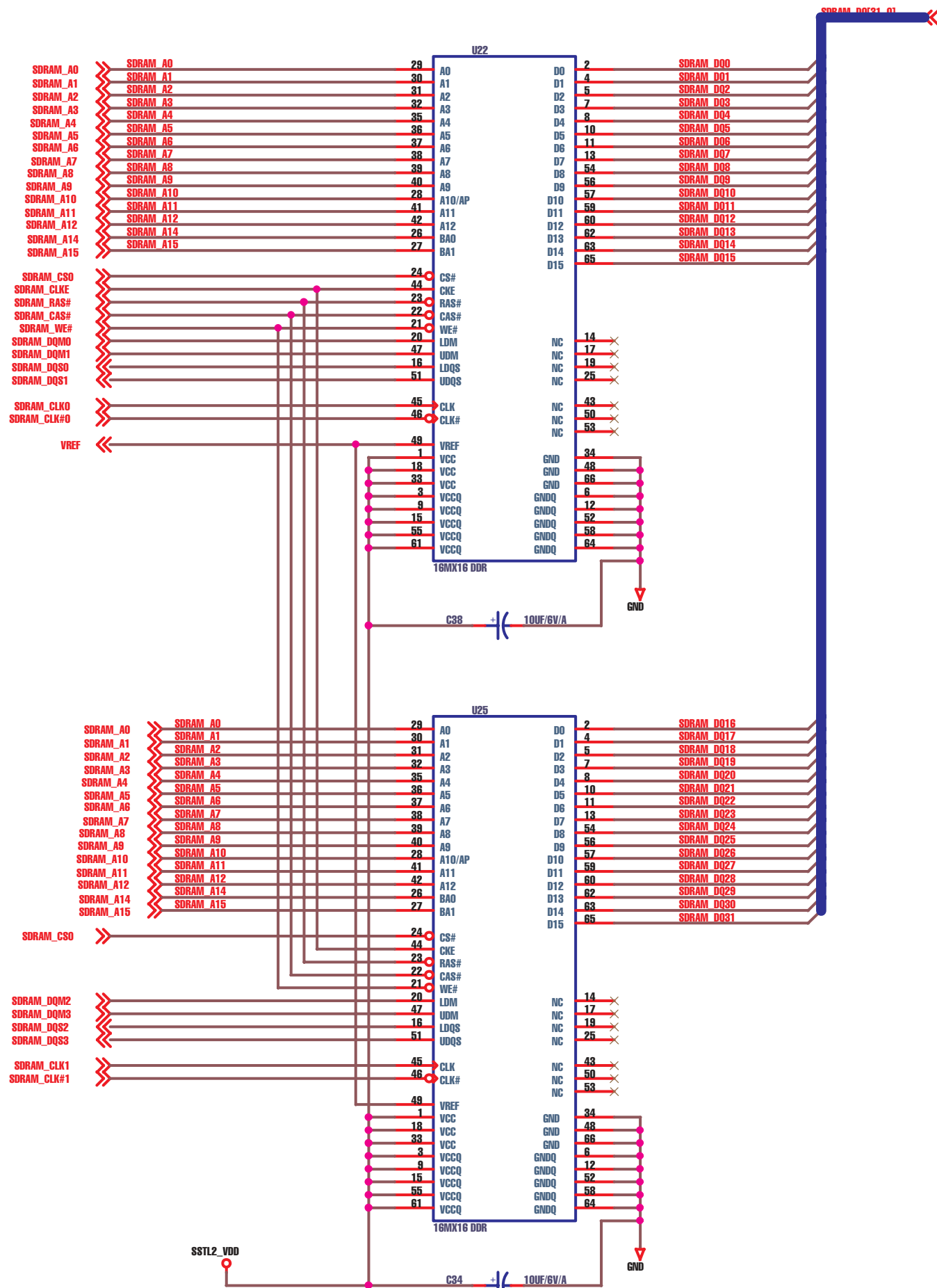


DDR TERMINATION VOLTAGE REGULATOR

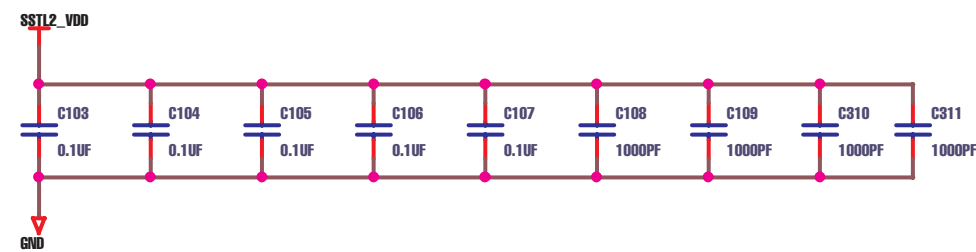
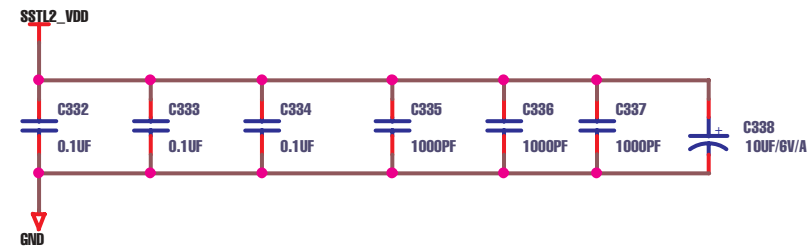
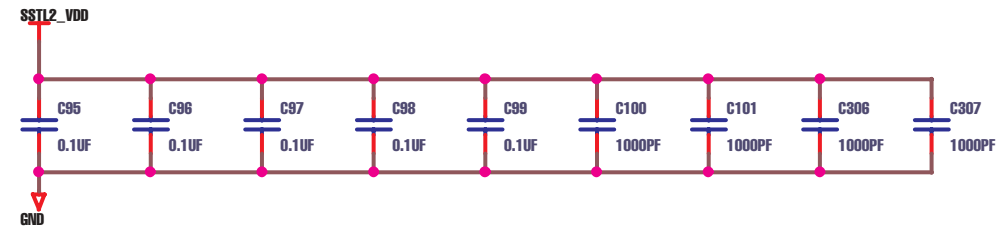
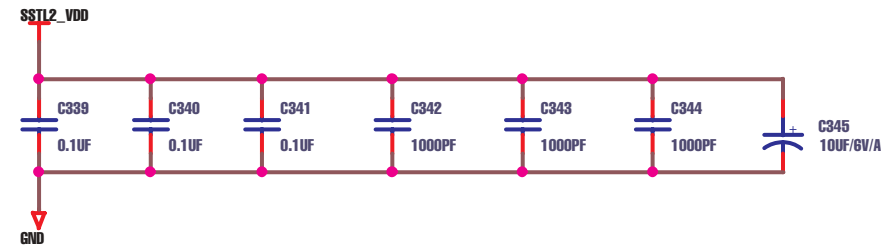
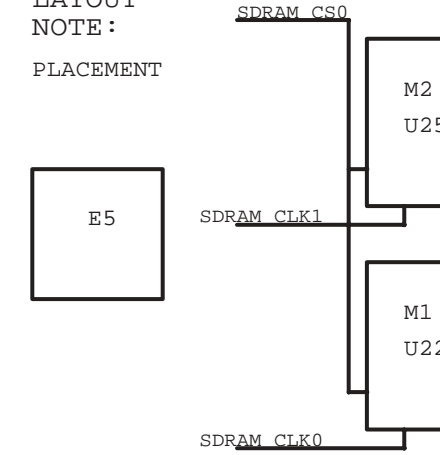
VREF needs to be decoupled to both SSSL2_VDD and SSSL2_GND with balanced decoupling capacitors.

VREF should be routed over a reference plane and isolated, and possibly shielded with both SSSL2_VDD and SSSL2_GND





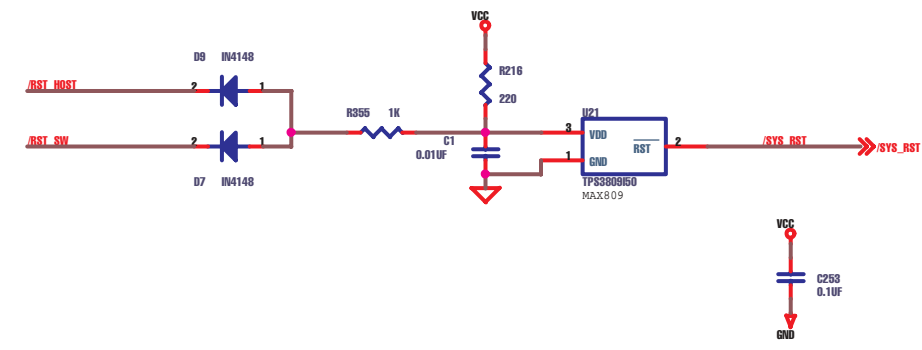
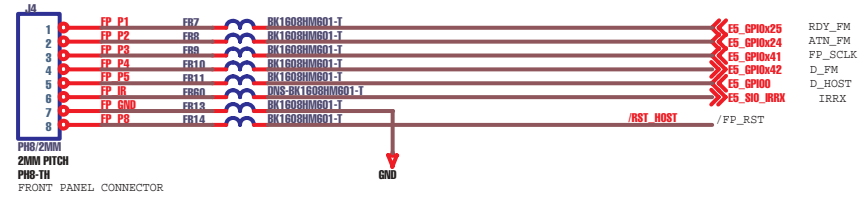
LAYOUT
NOTE :
PLACEMENT



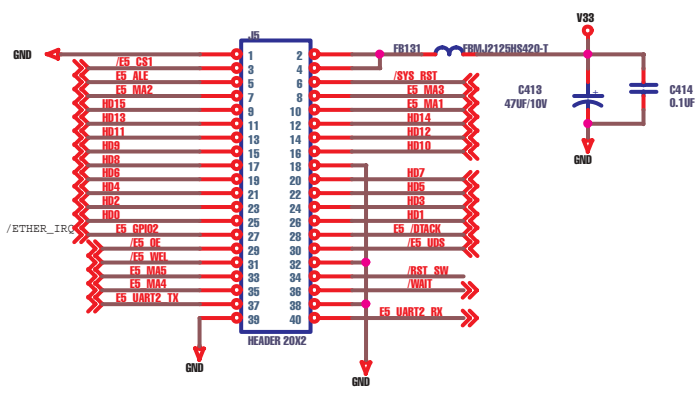
Revisão: A
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RESET CIRCUITRY

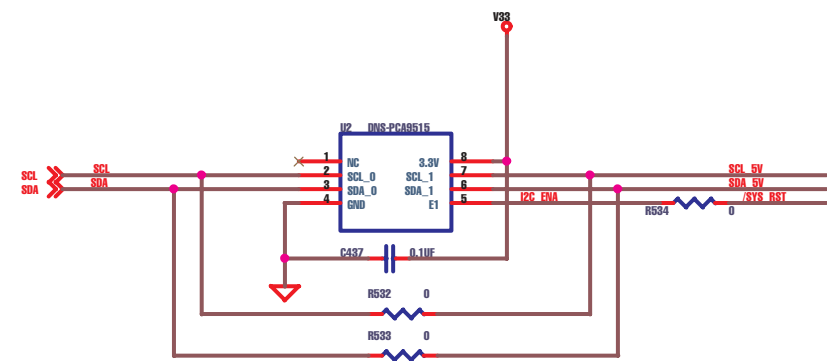
FRONT PANEL INTERFACE



E-Link IV Connector



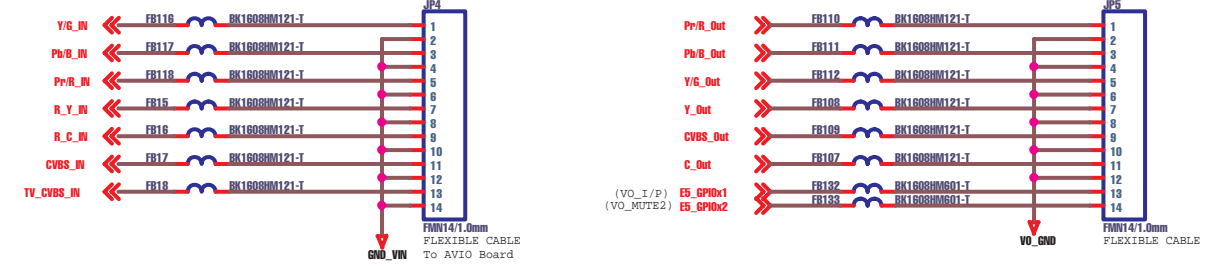
User can put a 10 pins 2MM header J8 without putting the 40 pins header JP7 for UART



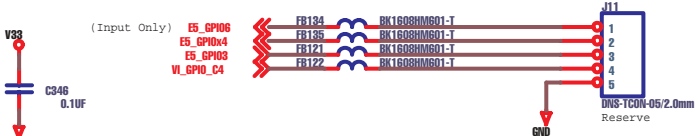
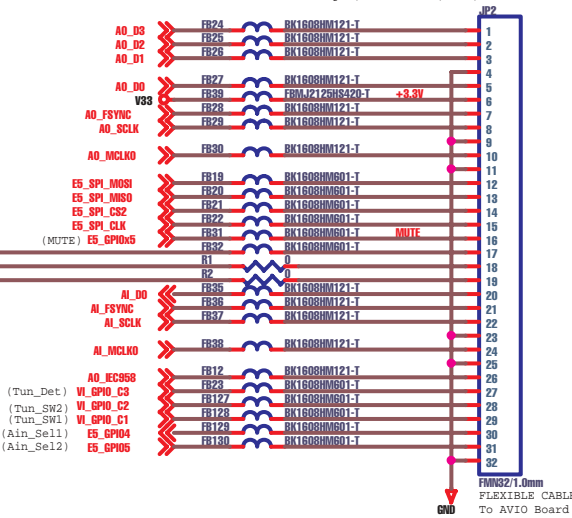
SCART Connector



A/V I/O Connector

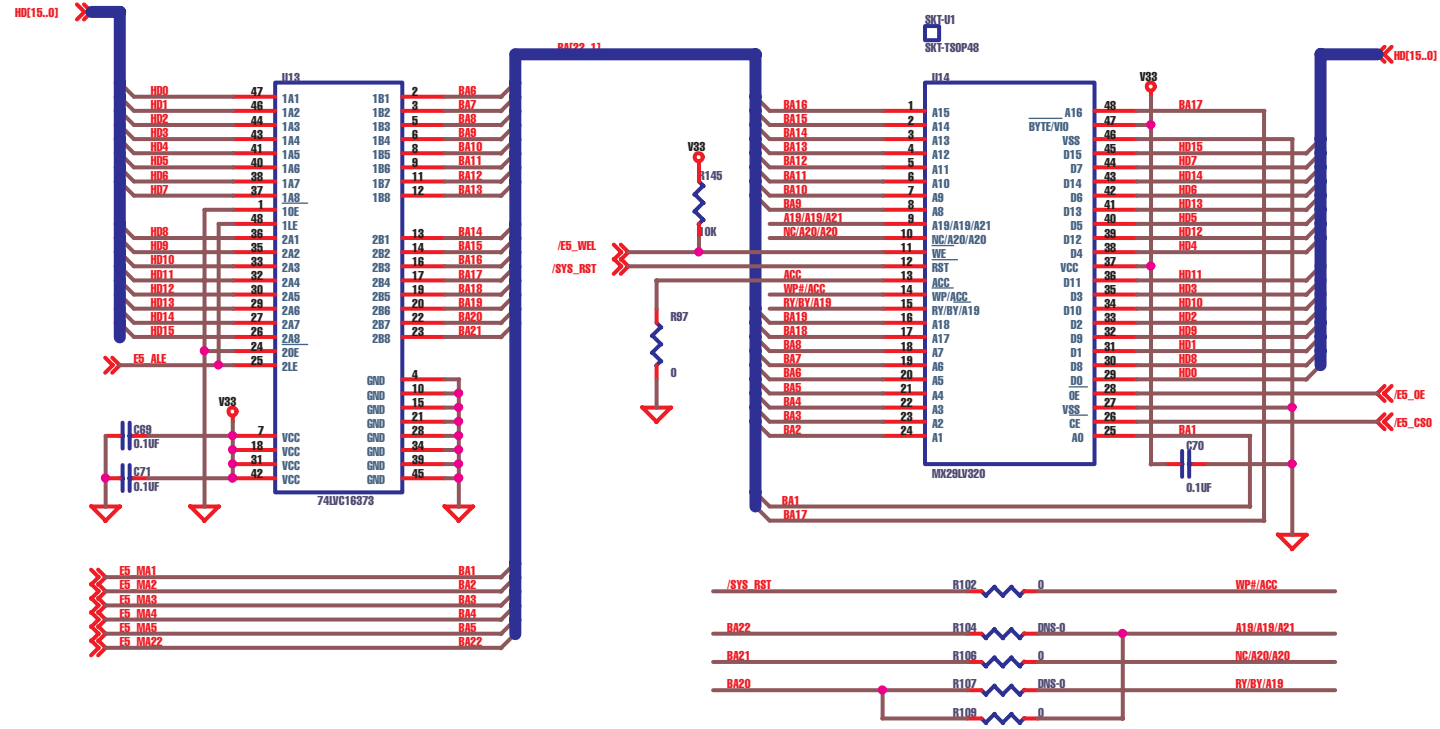
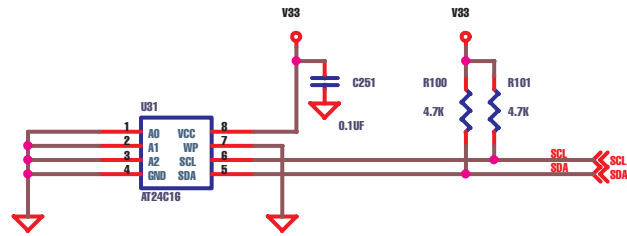
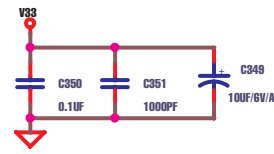
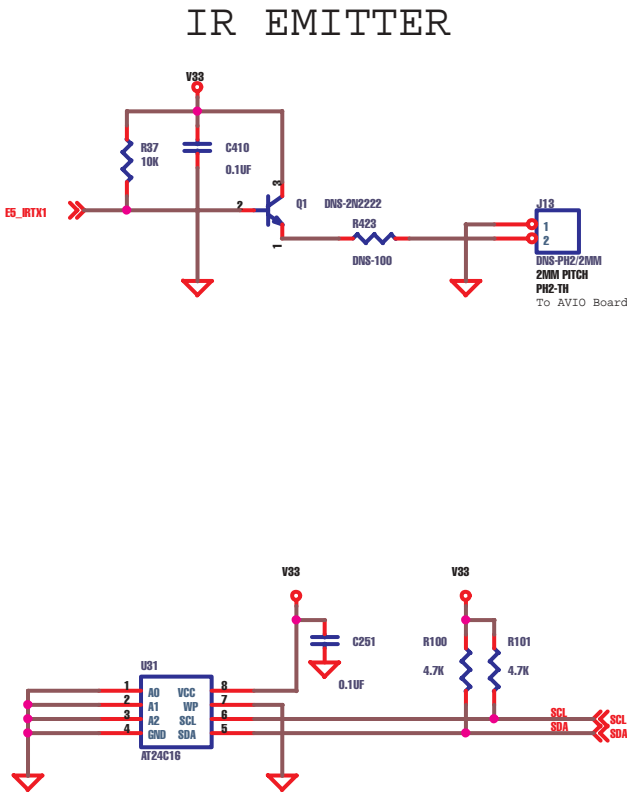


For Stereo audio output only, don't stuff FB24,FB25,FB26; JP2 use FMM24/1.0mm. For 5.1 channel audio output, stuff FB24,FB25,FB26; JP2 use FMM28/1.0mm.



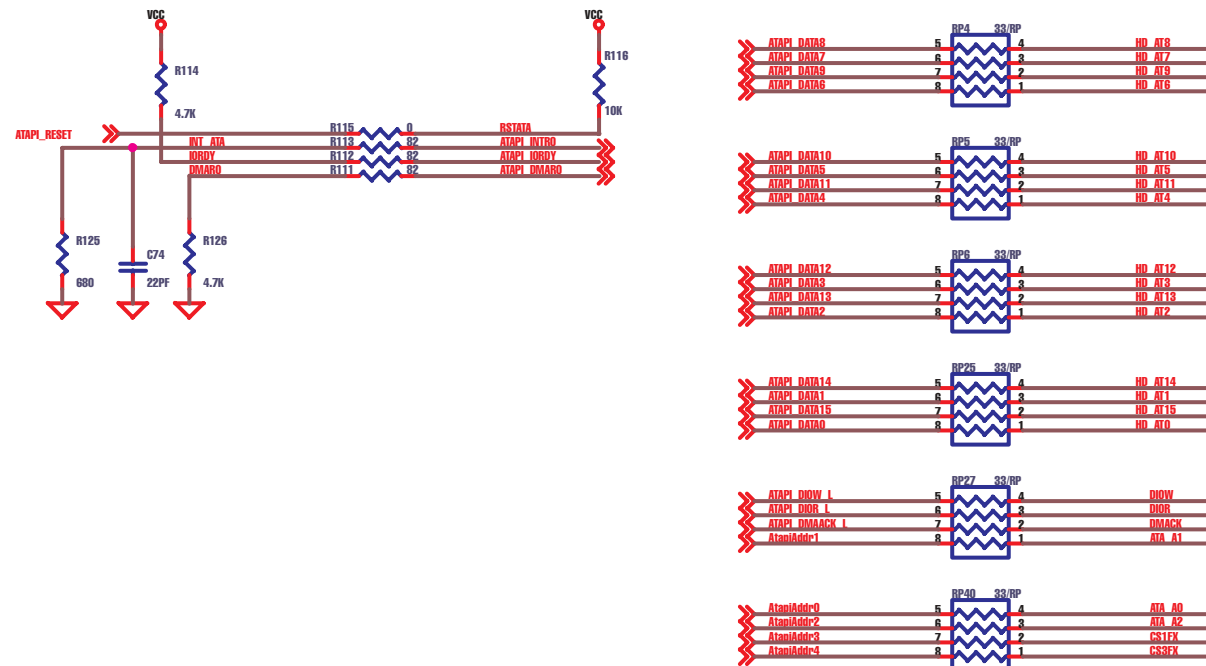
Revisão: A
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FLASH MEMORY(2 or 4 or 8 Mb)

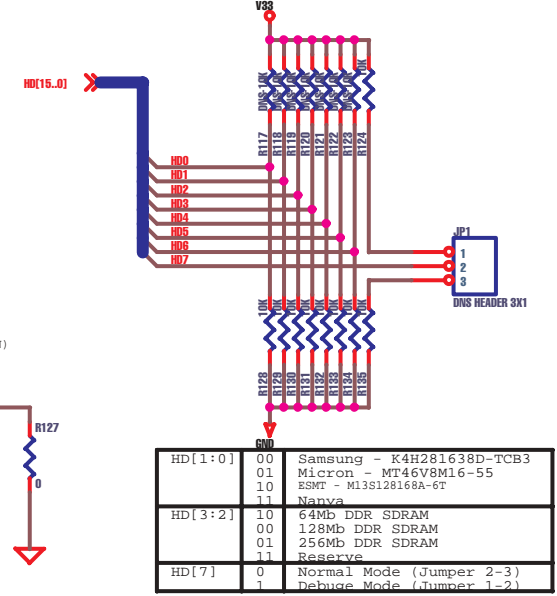


Size	Stuff	Not Stuff
1MB		R104,R106,R107,R109
2MB	R109	R104,R106,R107
4MB	R109,R106	R104,R107
8MB	R104,R106,R107	R109

DEDICATED ATAPI INTERFACE



HOST Read

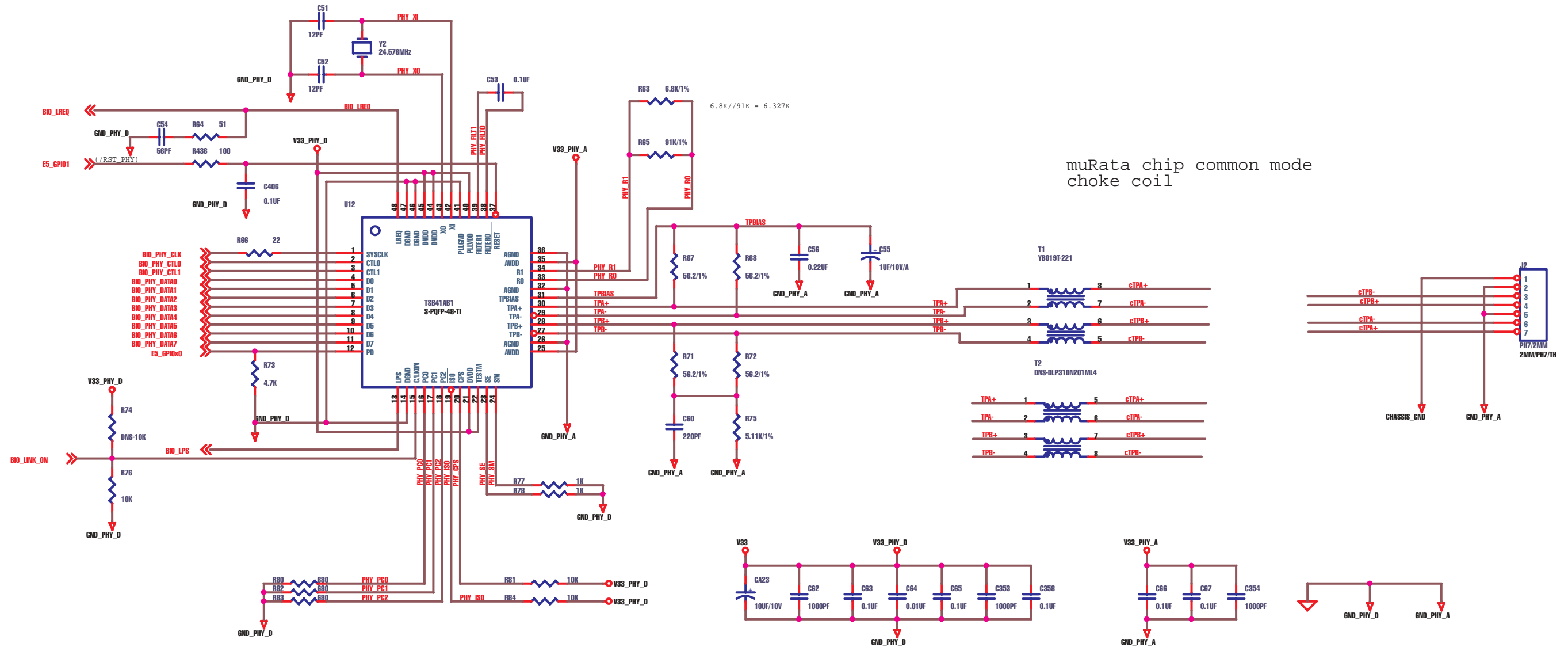


Header	Pin	Component
HD[1:0]	00	Samsung - K4H281638D-TCB3
	01	Micron - MT46V8M16-55
	10	ESMT - M13S128168A-6T
	11	Nanya
HD[3:2]	10	64Mb DDR SDRAM
	00	128Mb DDR SDRAM
	01	256Mb DDR SDRAM
	11	Reserve
HD[7]	0	Normal Mode (Jumper 2-3)
	1	Debug Mode (Jumper 1-2)

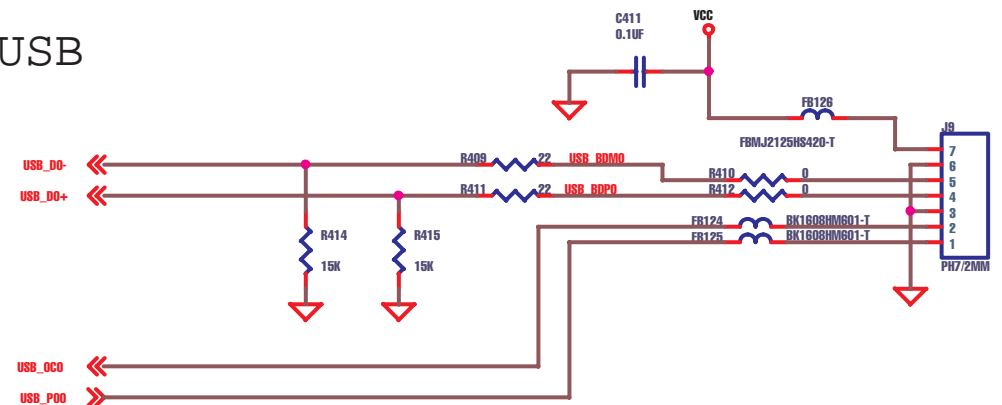
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FIREWIRE PHY

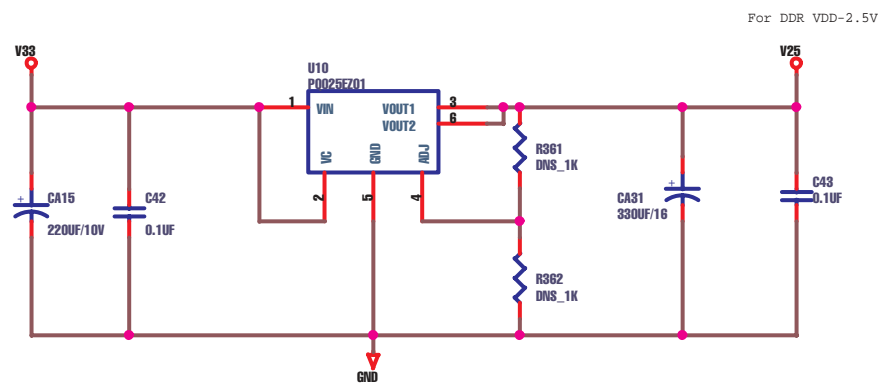
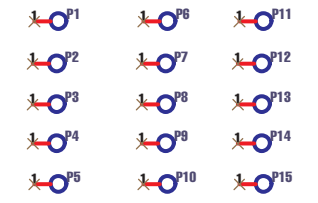
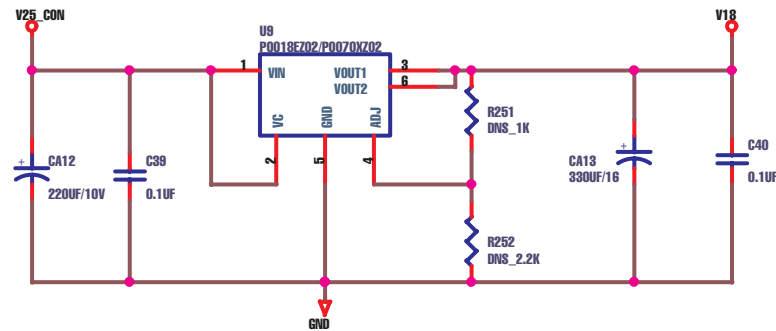
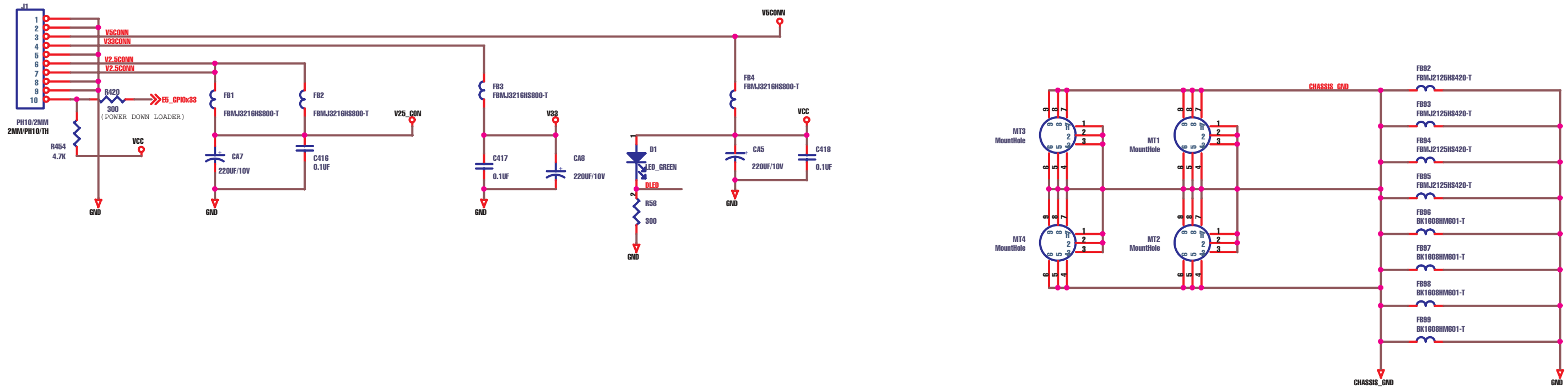


USB

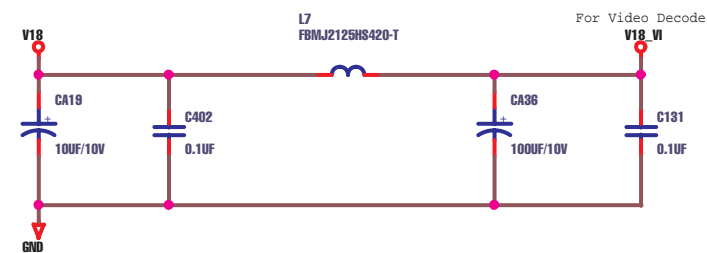


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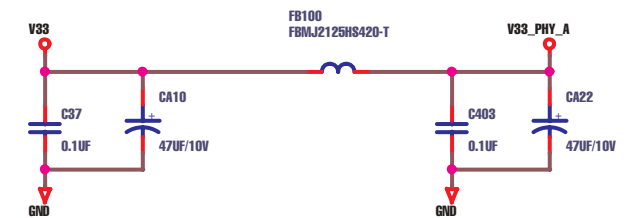
MAIN POWER CONN



For DDR VDD-2.5V

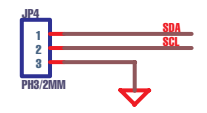
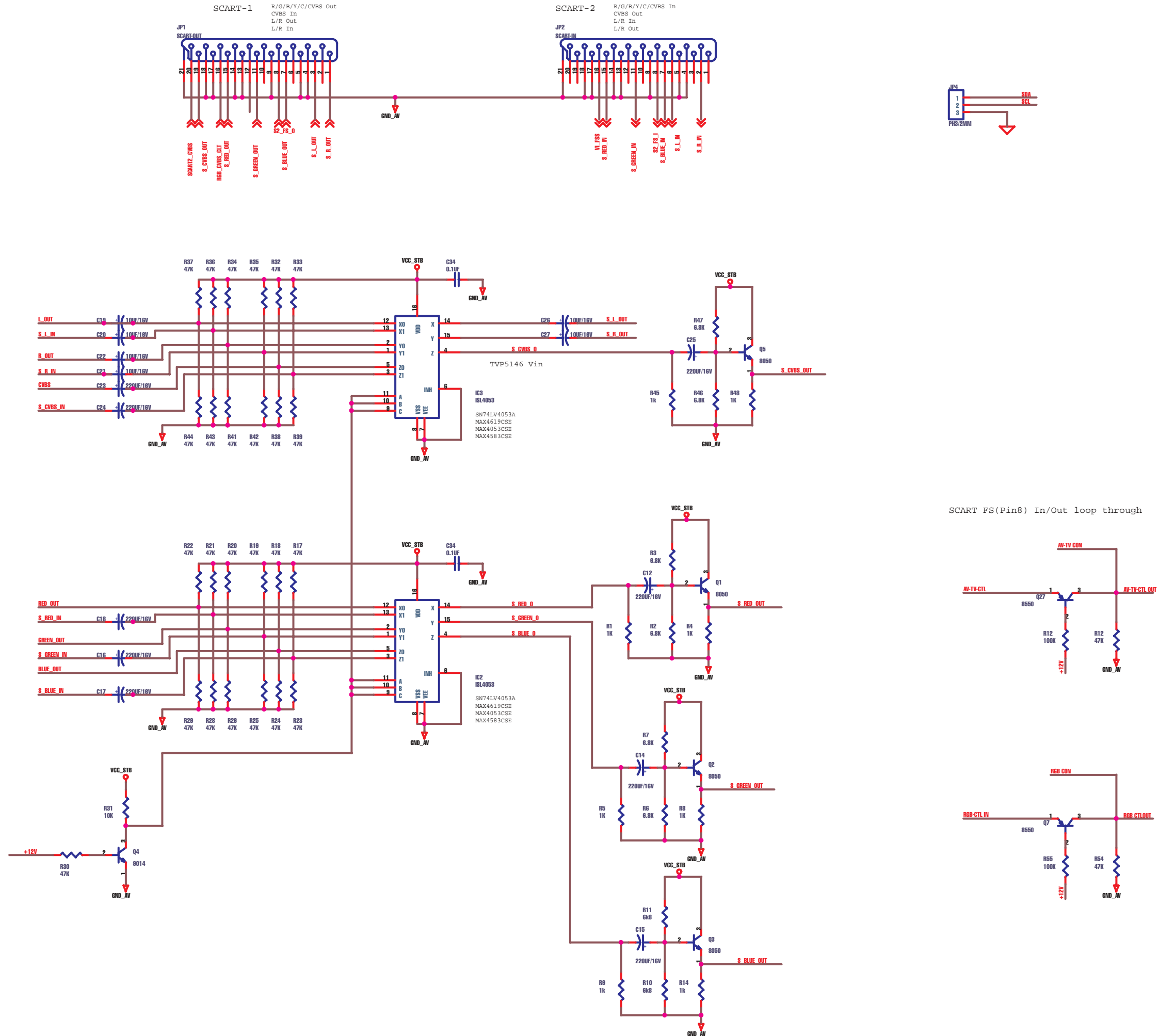


For Video Decode

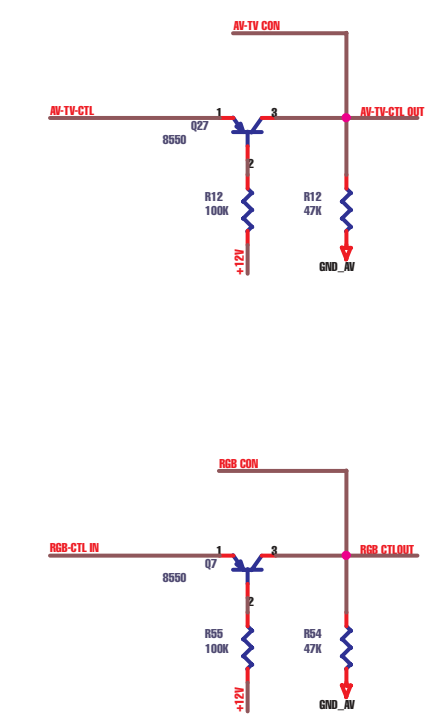


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ESQUEMA ELÉTRICO - DR-660



SCART FS(Pin8) In/Out loop through



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